

VI КОНФЕРЕНЦИЯ FPGA/RTL/Verification

FPGA-Systems 2024.1

Реализация контроллера SATA на ПЛИС

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Область применения интерфейса SATA

Накопители информации

- HDD
- SSD
- Оптические приводы



Варианты реализации контроллера SATA



ASIC



FPGA

Реализации на ПЛИС

В составе САПР

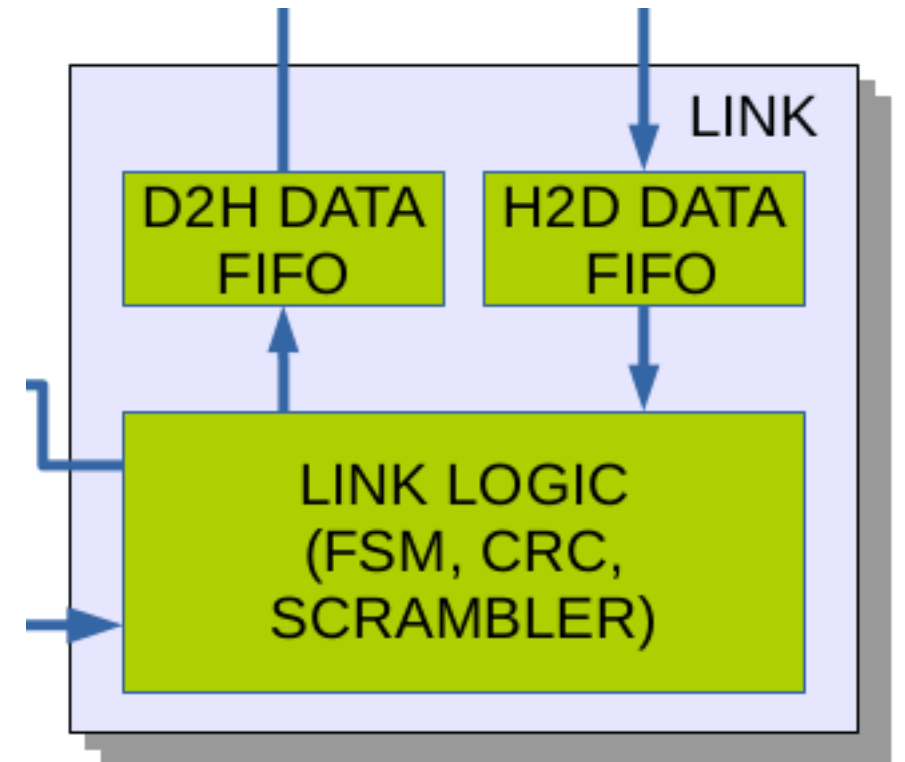
Project Summary x IP Catalog x

Cores | Interfaces

Search: sata (4 matches)

Name	AXI4	Status	License
Vivado Repository			
Alliance Partners			
Design-gateway			
SATA Host Controller IP Core		Production	Purchase
IntelliProp			
IntelliProp SATA ADICI Core	AXI4	Production	Purchase
IntelliProp SATA AHCI Core	AXI4	Production	Purchase
Design Gateway			
SATA Host Controller IP Core		Production	Purchase

С открытым кодом

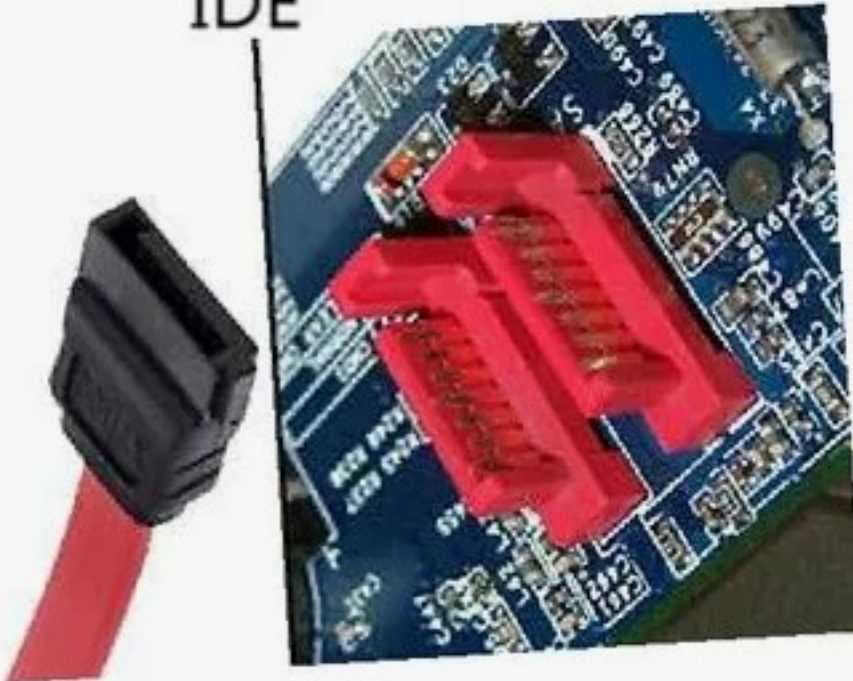


Эволюция интерфейса SATA



SATA

IDE



PATA

SATA

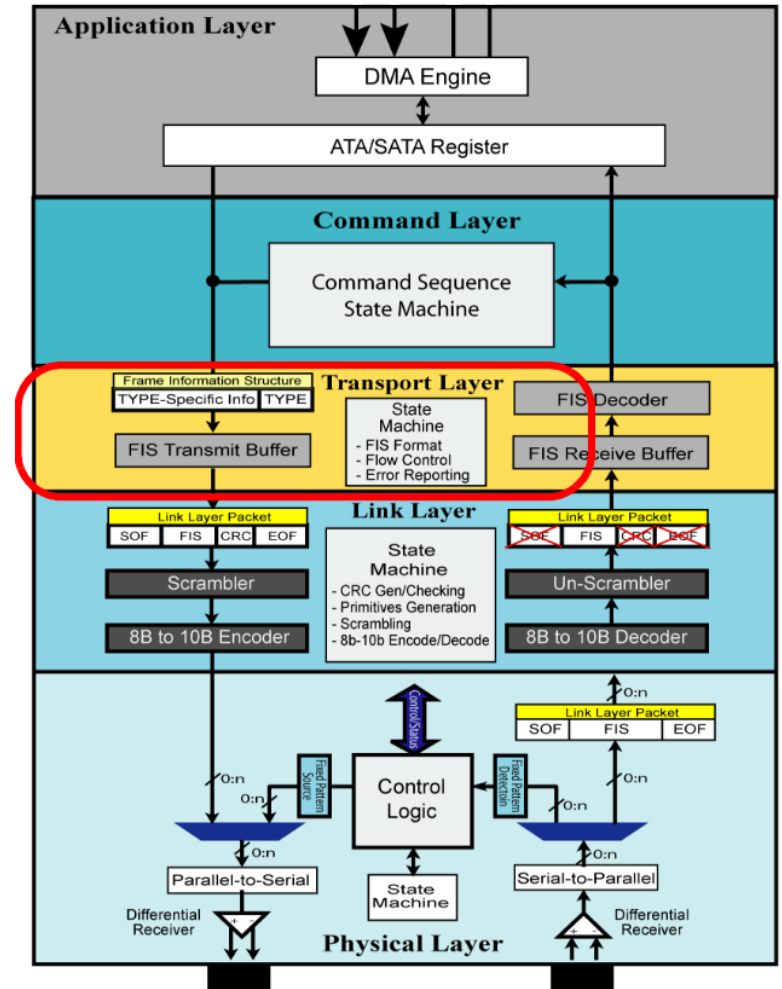
Литература

- Стандарт SATA. Serial ATA Revision 3.0
- Набор команд. ATA/ATAPI Command Set
- Устройство трансиверов
- Доп. литература, например “SATA Storage Technology”, Don Anderson, MindShare, Inc.



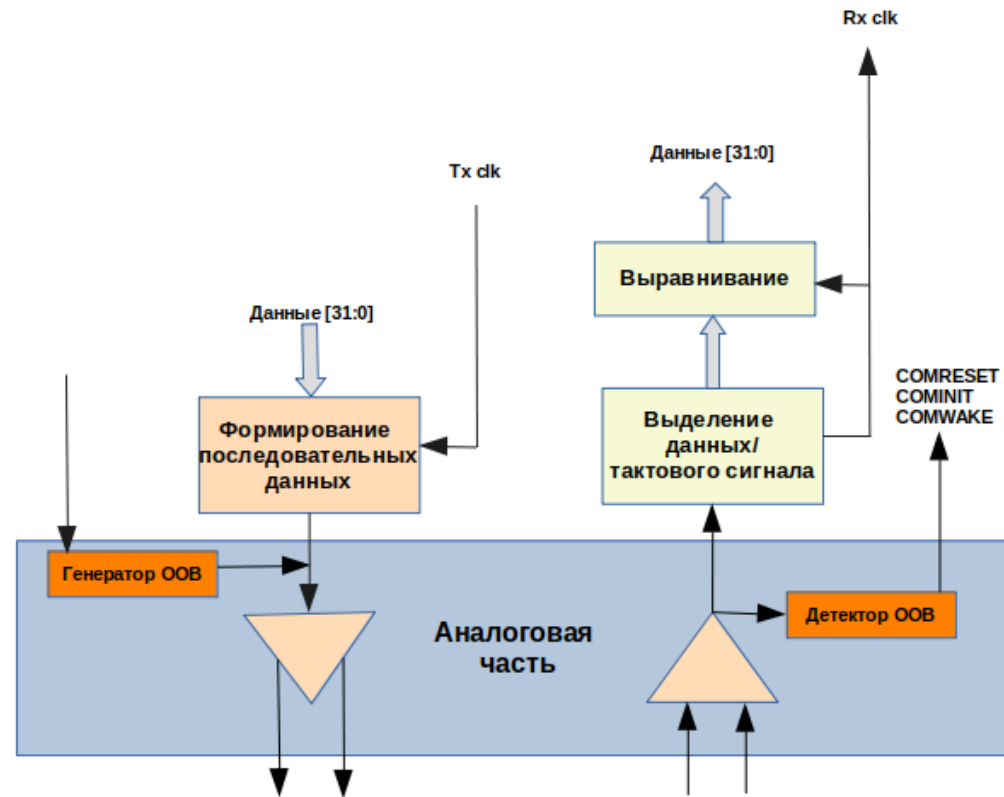
Уровни протокола SATA

- Уровень приложений
- Уровень команд
- Транспортный уровень
- Канальный уровень
- Физический уровень



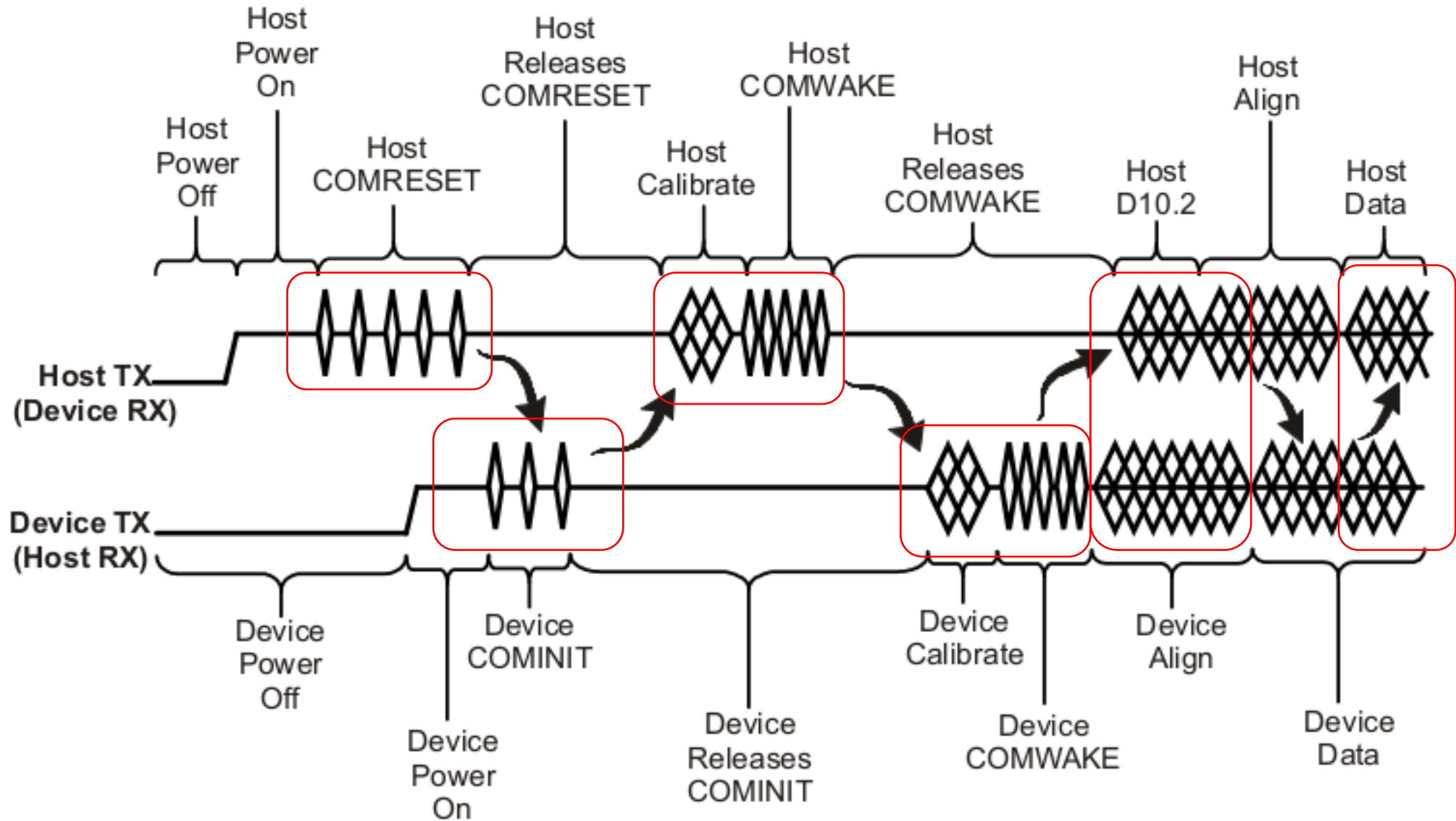
Физический уровень

- **Определение скорости – SATA1,2,3**
- **Последовательно – параллельное преобразование данных**
- **Тактовый сигнал со спектральной модуляцией (SSC)**

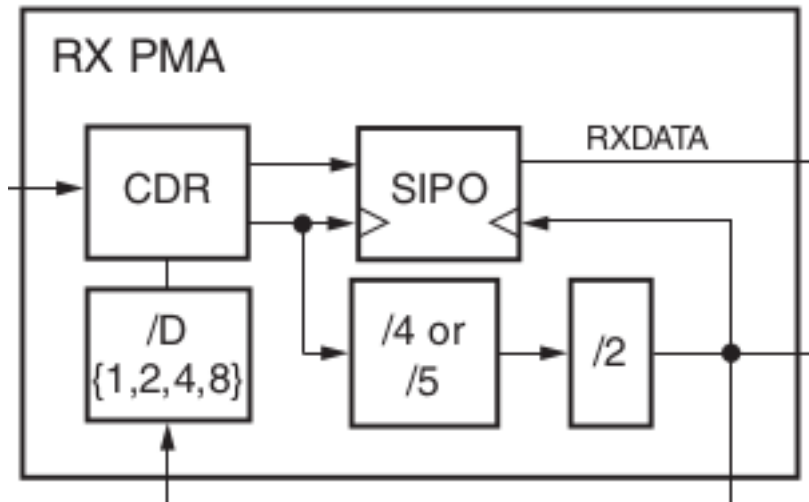


Как правило
выполняется на
трансиверах ПЛИС

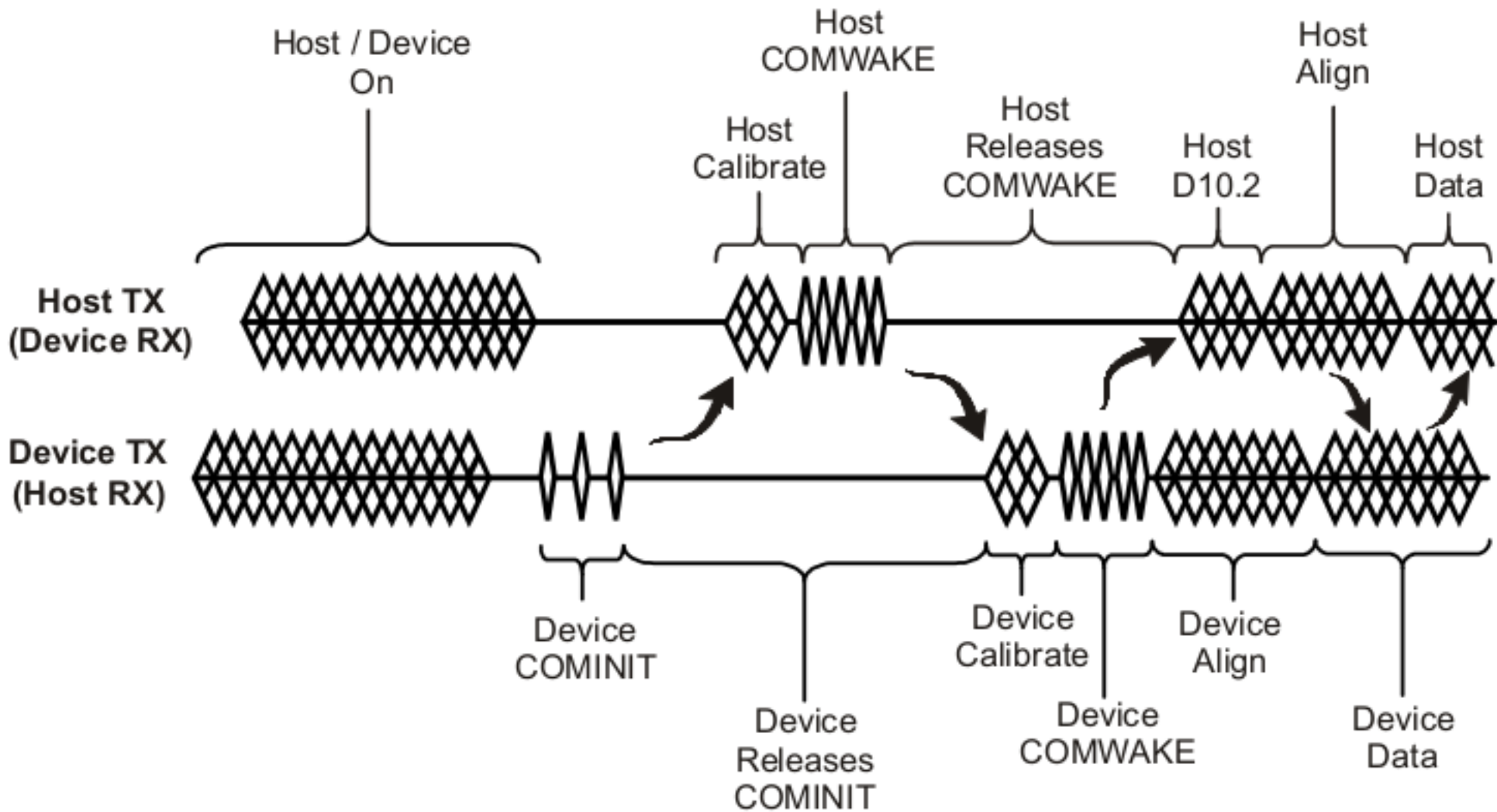
Out of Band Signaling



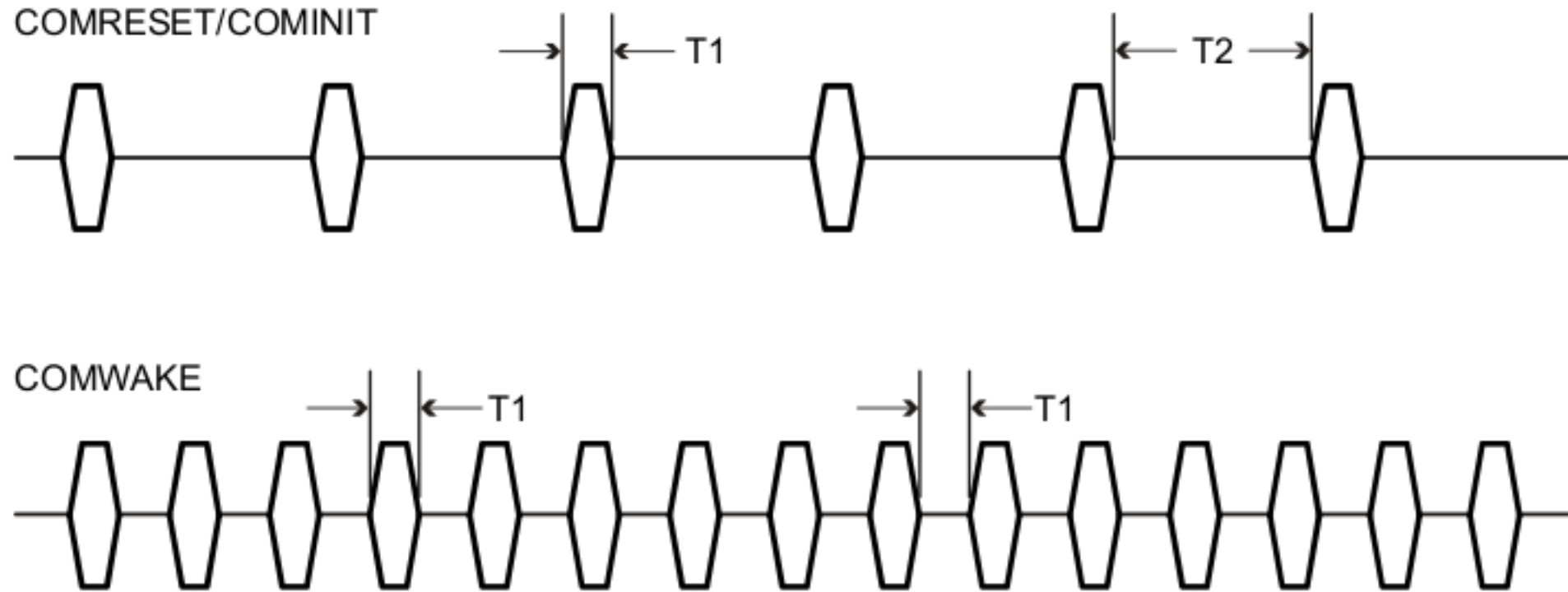
Где Rx CDR lock?



Последовательность COMINIT



Сигналы ООВ



Настройка трансивера

The image shows a software development environment with a code editor and a configuration wizard. The code editor displays Verilog code for RX OOB Signaling Attributes:

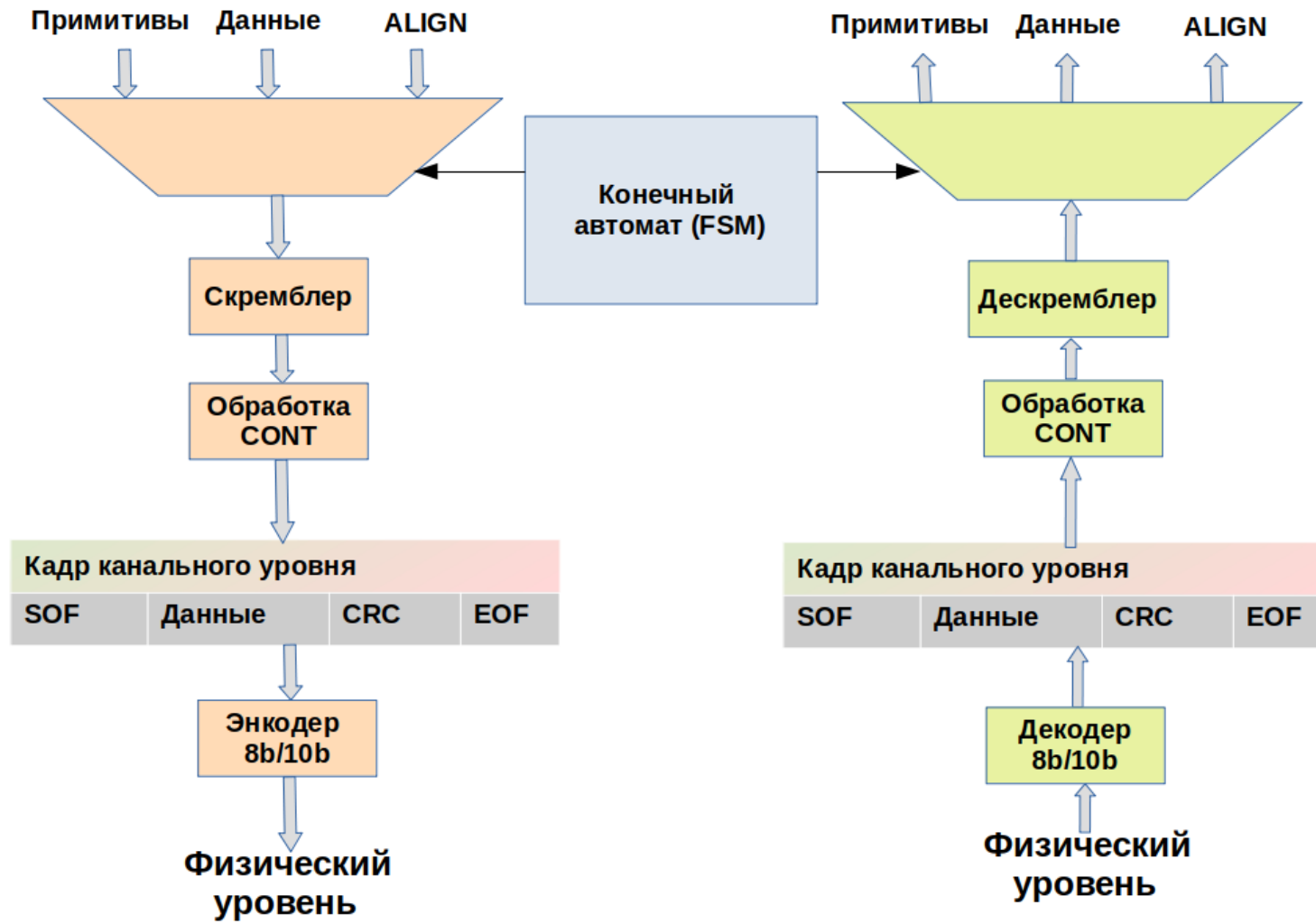
```
350 //-----RX OOB Signaling Attributes-----
351
352 .SAS_MAX_COM                (64),
353 .SAS_MIN_COM                (36),
354 .SATA_BURST_SEQ_LEN        (4'b0101), // def. value - (4'b0101),
355 .SATA_BURST_VAL            (3'b101), // def. value - (3'b111),
356 .SATA_IDLE_VAL            (3'b101), // def. value - (3'b111),
357 .SATA_MAX_BURST           (8),
358 .SATA_MAX_INT              (21)
```

The configuration wizard, titled "7 Series FPGAs Transceivers Wizard (3.6)", is currently on the "PCIe, SATA, PRBS" tab. It shows the following settings:

- Component Name: gtwizard_0
- GT Selection: Line Rate, RefClk Selection
- Encoding and Clocking
- Comma Alignment and Equalization
- PCIe, SATA, PRBS (selected)
- CB and CC Sequence
- Summary

Under the "PCIe Express and SATA" section, the "Enable PCI Express" checkbox is unchecked. Under the "SATA COM sequence" section, the "Bursts" and "Idles" fields are both set to 7, with a range of [0 - 7] indicated next to each field.

Канальный уровень



Конечный автомат канального уровня

LT1: HL_SendChkRdy		Transmit X_RDY _p .	
1. R_RDY _p received from Phy.	→	L_SendSOF	
2. X_RDY _p received from Phy.	→	L_RcvWaitFifo	
3. AnyDword other than (R_RDY _p or X_RDY _p) ¹ received from Phy layer.	→	HL_SendChkRdy	
4. PHYRDYn	→	L_NoCommErr ²	
NOTES:			
1. Any received errors such as 10b decoding errors and invalid primitives are ignored.			
2. The Link layer shall notify the Transport layer of the condition and fail the attempted transfer.			

LT2: DL_SendChkRdy		Transmit X_RDY _p .	
1. R_RDY _p received from Phy.	→	L_SendSOF	
2. AnyDword other than R_RDY _p received from Phy.	→	DL_SendChkRdy	
3. PHYRDYn	→	L_NoCommErr	



Примитивы канального уровня

Primitive Name	Byte 3 Contents	Byte 2 Contents	Byte 1 Contents	Byte 0 Contents
ALIGN _P	D27.3	D10.2	D10.2	K28.5
CONT _P	D25.4	D25.4	D10.5	K28.3
DMAT _P	D22.1	D22.1	D21.5	K28.3
EOF _P	D21.6	D21.6	D21.5	K28.3
HOLD _P	D21.6	D21.6	D10.5	K28.3
HOLDA _P	D21.4	D21.4	D10.5	K28.3
PMACK _P	D21.4	D21.4	D21.4	K28.3
PMNAK _P	D21.7	D21.7	D21.4	K28.3
PMREQ_P _P	D23.0	D23.0	D21.5	K28.3
PMREQ_S _P	D21.3	D21.3	D21.4	K28.3
R_ERR _P	D22.2	D22.2	D21.5	K28.3
R_IP _P	D21.2	D21.2	D21.5	K28.3
R_OK _P	D21.1	D21.1	D21.5	K28.3
R_RDY _P	D10.2	D10.2	D21.4	K28.3
SOF _P	D23.1	D23.1	D21.5	K28.3
SYNC _P	D21.5	D21.5	D21.4	K28.3
WTRM _P	D24.2	D24.2	D21.5	K28.3
X_RDY _P	D23.2	D23.2	D21.5	K28.3

Пример транзакции канального уровня

Transmitter	Receiver
XXXX	XXXX
XXXX	XXXX
X_RDY _p	XXXX
X_RDY _p	XXXX
CONT _p	XXXX
XXXX	XXXX
XXXX	R_RDY _p
XXXX	R_RDY _p
XXXX	CONT _p
SOF _p	XXXX
DATA (FIS Type)	XXXX
DATA	XXXX
DATA	R_IP _p
DATA	R_IP _p
DATA	CONT _p
HOLD _p	XXXX
HOLD _p	XXXX
CONT _p	XXXX
XXXX	XXXX
XXXX	HOLDA _p
XXXX	HOLDA _p

Transmitter	Receiver
HOLD _p	CONT _p
DATA	XXXX
DATA	XXXX
DATA	XXXX
CRC	XXXX
EOF _p	R_IP _p
WTRM _p	R_IP _p
WTRM _p	CONT _p
WTRM _p	XXXX
CONT _p	XXXX
XXXX	R_OK _p
XXXX	R_OK _p
XXXX	CONT _p
XXXX	XXXX
SYNC _p	XXXX
SYNC _p	XXXX
CONT _p	XXXX
XXXX	XXXX
XXXX	SYNC _p
XXXX	SYNC _p
XXXX	CONT _p
XXXX	XXXX
XXXX	XXXX

Транспортный уровень

- **Обеспечивает прием/передачу фреймов**
- **Каждый фрейм имеет свой формат**
- **Наборы фреймов для хоста и устройства различаются**
- **Два основных режима передачи – DMA и FPDMA**

Type field value	Description
27h	Register FIS – Host to Device
34h	Register FIS – Device to Host
39h	DMA Activate FIS – Device to Host
41h	DMA Setup FIS – Bi-directional
46h	Data FIS – Bi-directional
58h	BIST Activate FIS – Bi-directional
5Fh	PIO Setup FIS – Device to Host
A1h	Set Device Bits FIS – Device to Host

0	Features(7:0)	Command	C	R	R	R	PM Port	FIS Type (27h)
1	Device	LBA(23:16)	LBA(15:8)				LBA(7:0)	
2	Features(15:8)	LBA(47:40)	LBA(39:32)				LBA(31:24)	
3	Control	ICC 7 6 5 4 3 2 1 0	Count(15:8)				Count(7:0)	
4	Reserved (0)	Reserved (0)	Reserved (0)				Reserved (0)	

Примеры транзакций DMA

	Read DMA Ext			Write DMA Ext	
	Host	Device		Host	Device
0x00258027	0x00258027			0x00358027	
0x27 – Register FIS	0x4000010e		LBA	0x4000010e	
0x80 – Flags	0x00000000		LBA	0x00000000	
0x25 – Command	0x00000002		Count	0x00000002	
0x00 – Features	0x00000000			0x00000000	
0x00000046		0x00000046			0x00504034
0x46 – Data FIS		...			0x4000010e
					0x00000000
0x00504034		0x00504034			0x02000000
0x34 – Register FIS		0x4000010e			0x00000000
0x40 – Flags		0x00000000			
0x50 – Status		0x00000002		0x00000046	
0x00 – Error		0x00000000		...	
					0x00504034
					...

Режим FRDMA – чтение

0x60 – Read FPMA Queued		
Host	Device	
0x08608027		0x08 – Size in blocks
0x40706a20		0x27 – Register Host to Device
0x00000074		
0x08000028		[7:3] – NCQ tag (5)
0x00000000		
	0x00400034	0x34 – Register – Device to Host
	0x40706a20	
	0x00000074	
	0x00000028	
	0x00000000	
	0x00002041	0x41 – DMA Setup
	0x00000005	NCQ tag
	0x00000000	
	0x00000000	
	0x00001000	Size in bytes
	0x00000000	
	0x00000046	0x46 – Data
	...	
	0x004040a1	0xA1 – Set Device Bits
	0x00000020	tag 5 device bits

0	Features(7:0)	Command	C R R R	PM Port	FIS Type (27h)
1	Device	LBA(23:16)		LBA(15:8)	LBA(7:0)
2	Features(15:8)	LBA(47:40)		LBA(39:32)	LBA(31:24)
3	Control	ICC 7 6 5 4 3 2 1 0		Count(15:8)	Count(7:0)
4	Reserved (0)	Reserved (0)		Reserved (0)	Reserved (0)

Word	Name	Description
00h	Feature	The number of logical sectors to be transferred. A value of 0000h indicates that 65,536 logical sectors are to be transferred.
01h	Count	Bit Description 15:8 Reserved 7:3 NCQ Tag - See 6.3.3 2:0 Reserved
02h	LBA	(MSB) _____ Address of the first logical sector to be transferred. _____ (LSB)
03h		
04h		
05h	Device	Bit Description 15 FUA - See 7.28.3.2 14 Shall be set to one 13 Reserved 12 Shall be set to zero 11:8 Reserved
	Command	7:0 60h

Режим FPDMA - запись

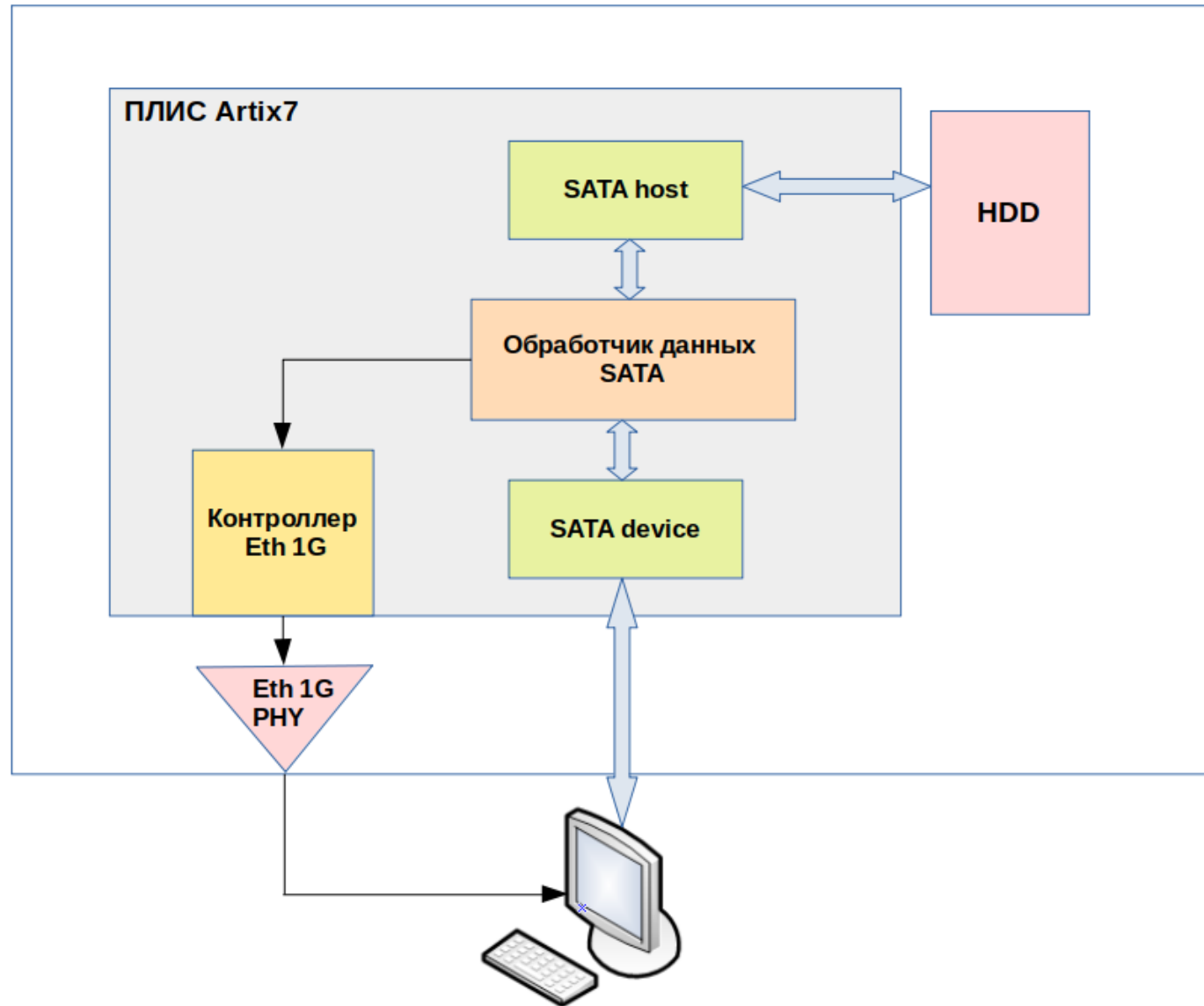
0x61 - Write FPMA Queued		
Host	Device	
0x40618027		0x40 - Size in blocks 0x27 - Register Host to Device
0x40808900		
0x0500005d		
0x080000a8		[7:3] - NCQ tag (0x15)
0x00000000		
	0x00400034	0x34 - Register - Device to Host
	0x40808900	
	0x0000005d	
	0x000000a8	
	0x00000000	
	0x00008041	0x41 - DMA Setup
	0x00000015	NCQ tag
	0x00000000	
	0x00000000	
	0x00000000	
	0x000a8000	Size in bytes
	0x00000000	
0x00000046		0x46 - Data
...		
	0x00000039	0x39 - DMA Activate
0x00000046		
...		
	0x00000039	
0x00000046		
...	...	Передача всех блоков данных
0x00000046		
...		
	0x004040a1	0xa1 - Set Device Bits
	0x00200000	Device bits for tag 0x15

0	Reserved (0)	Reserved (0)	A	I	D	R	PM Port	FIS Type (41h)
1	DMA Buffer Identifier Low							
2	DMA Buffer Identifier High							
3	Reserved (0)							
4	DMA Buffer Offset							
5	DMA Transfer Count							
6	Reserved (0)							

0	Reserved (0)	Reserved (0)	R	R	R	R	PM Port	FIS Type (39h)
---	--------------	--------------	---	---	---	---	---------	----------------

0	Error	R	Status Hi	R	Status Lo	N	I	R	R	PM Port	FIS Type (A1h)
1	Protocol Specific										

Целевое устройство



- **Реализация ООВ для трансиверов GTP – недостаточно времени для синхронизации.**
- **Необходимость методов контроля синхронизации Rx CDR**
- **Настройки трансивера для SATA - количество импульсов ООВ**
- **Приоритеты на передачу устройства и хоста на канальном уровне**
- **Размер блока данных на транспортном уровне для пакета 0x46**
- **Высокоуровневая отладка с помощью Ethernet 1G и Wireshark**



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