Плисы, Наука, Зачем?

Или жизнь FPGA в научной среде

Александр Бойков

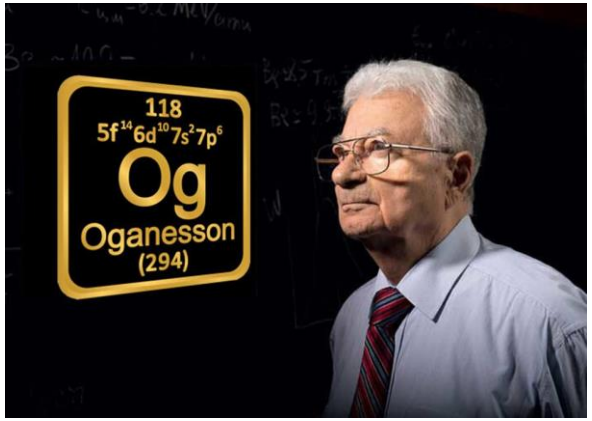
Дисклеймер

- Материал скорее популярный, чем технический
- Мнение автора может не совпадать с мнением коллег
- Тут нет UVM, Cocotb и.т.д.
- Впереди 17 слайдов

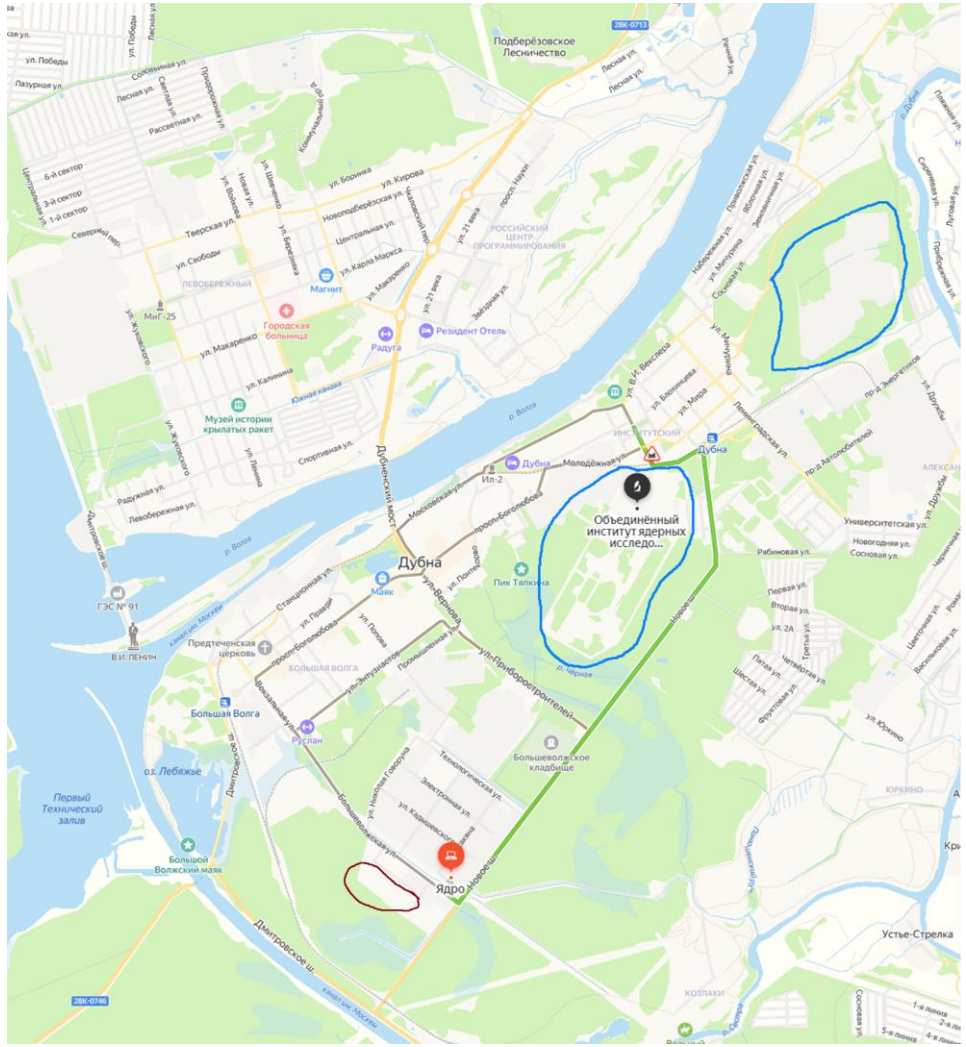
- Многое распространяется под лицензиями CERN OHL-*(P/W/S)*
- Ссылки на источники будут за QR-кодами

ОИЯИ/JINR

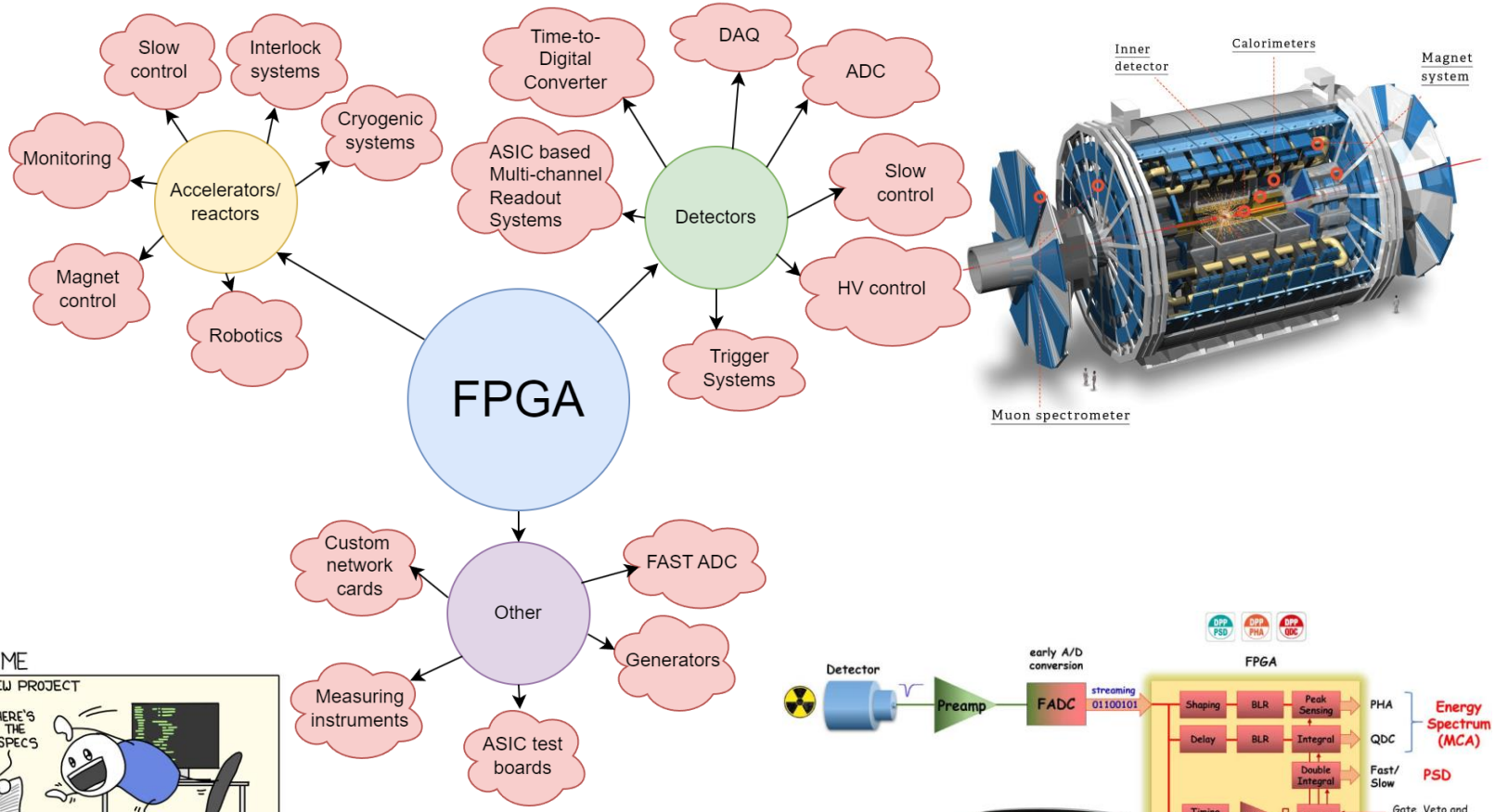
Объединенный институт ядерных исследований — международная межправительственная научно-исследовательская организация, созданная на основе Соглашения, подписанного одиннадцатью странами-учредителями *26 марта 1956 г.*



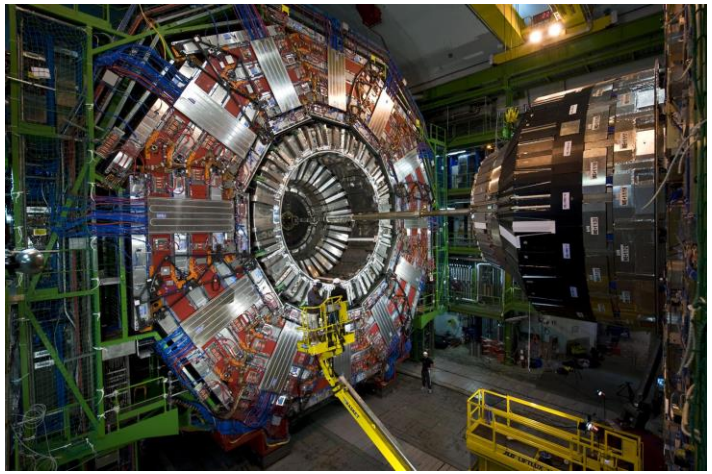
В ОИЯИ синтезировали элементы завершающие седьмой период таблицы Менделеева: 114 (флеровий), 115 (московий), 116 (ливерморий), 117 (теннессин) и 118 (оганесон)

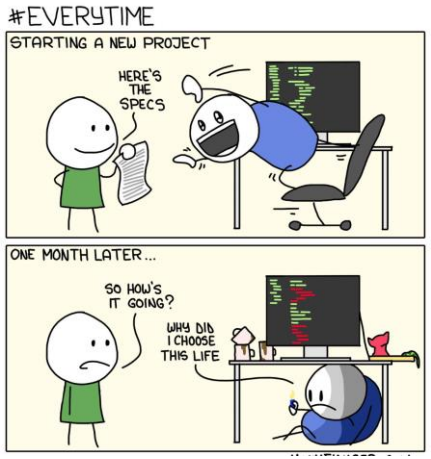


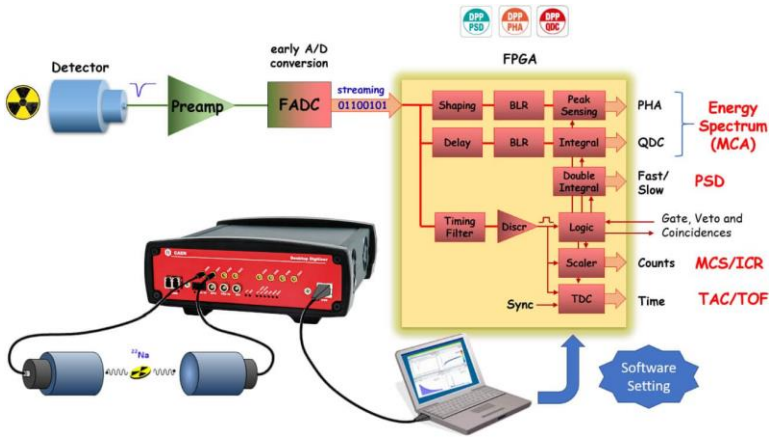
Мейнстрим


FPGA
Accelerators/ reactors
Slow control
Interlock systems
Cryogenic systems
Monitoring
Magnet control
Robotics
Detectors
Time-to-Digital Converter
DAQ
ADC
ASIC based Multi-channel Readout Systems
Slow control
HV control
Trigger Systems
Other
Custom network cards
FAST ADC
Generators
Measuring instruments
ASIC test boards

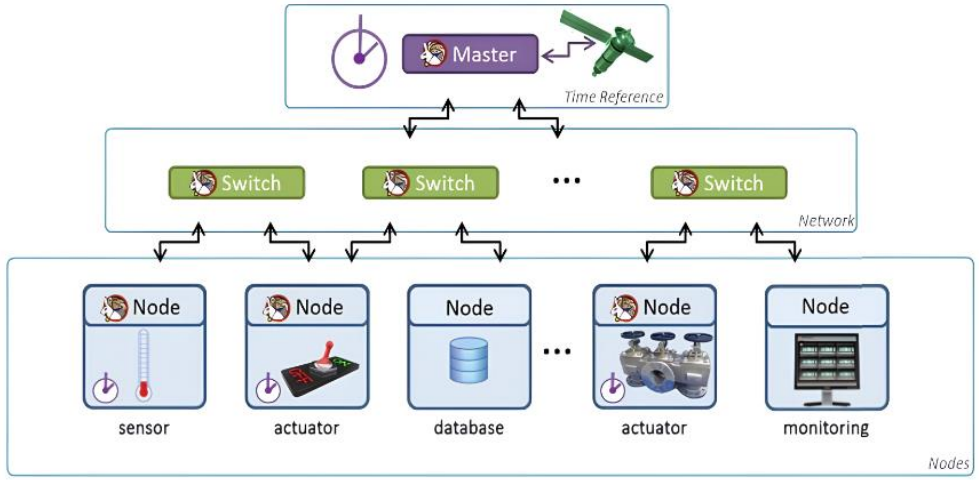
Inner detector
Calorimeters
Magnet system
Muon spectrometer




#EVERYTIME
STARTING A NEW PROJECT
HERE'S THE SPECS
ONE MONTH LATER...
SO HOW'S IT GOING?
WHY DID I CHOOSE THIS LIFE

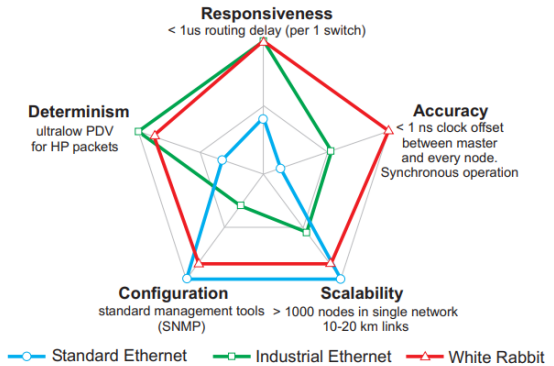

Detector
Preamp
early A/D conversion
FADC
streaming
01100101
FPGA
Shaping
BLR
Peak Sensing
PHA
Delay
BLR
Integral
QDC
Energy Spectrum (MCA)
Double Integral
Fast/ Slow
PSD
Timing Filter
Discr
Logic
Gate, Veto and Coincidences
Scaler
Counts
MCS/ICR
Sync
TDC
Time
TAC/TOF
Software Setting

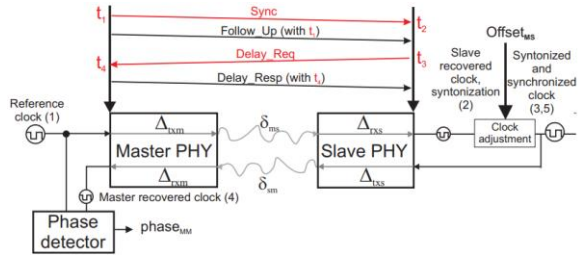
Кролик

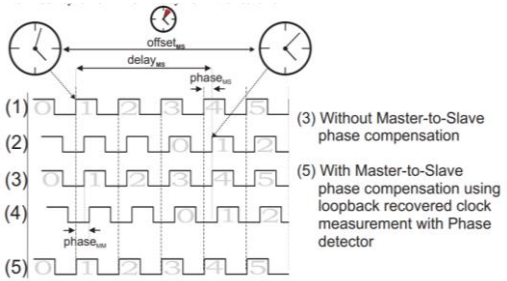


SCAN ME

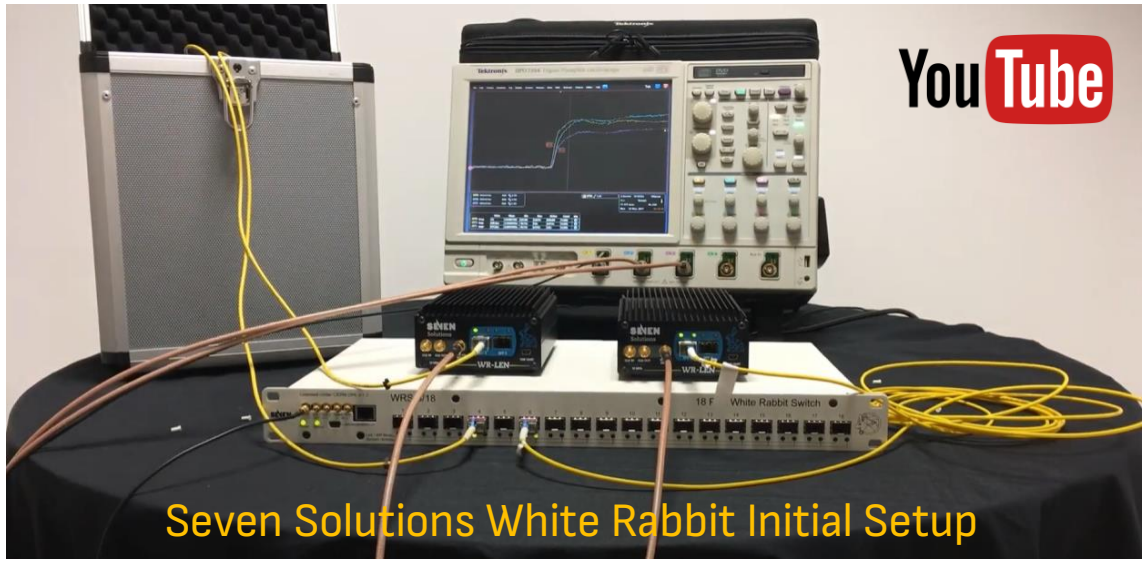
The White Rabbit Project







- Синхронизация с точностью 1 Нс или лучше
- Стабильно поддерживает сети с длиной связи до 10 Км (VTT MIKES успешно достиг 1000км с точностью 50нс)
- *Потенциально* нет ограничений в размере сети
- Доступны исходники IP и документация (лицензия)
- Поднимали на Virtex-6, Artix-7, UltraScale+… (более 10 платформ)



Кролик. Зачем?

ПОЛИТЕХ
Санкт-Петербургский политехнический университет Петра Великого

SCAN ME

CERN The White Rabbit Project

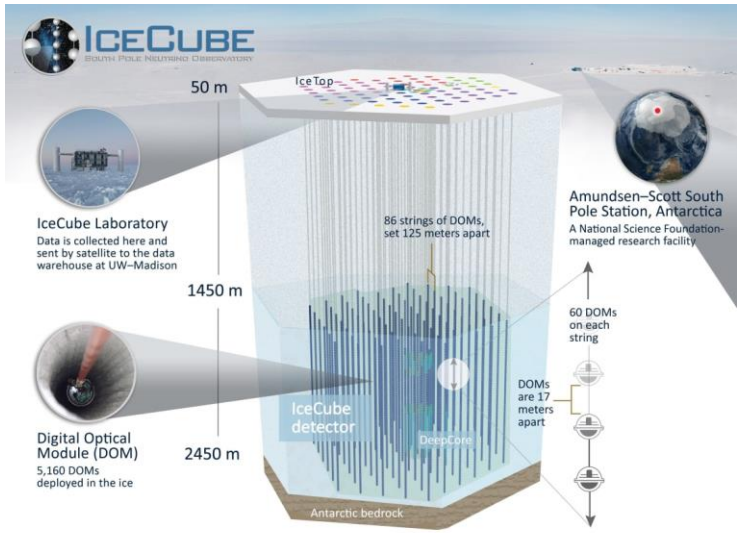
Физика высоких энергий

NICA (Nuclotron based Ion Collider fAcility), JINR, Russia

LHC (Large Hadron Collider), CERN, Switzerland

Астрономия (телескопы)

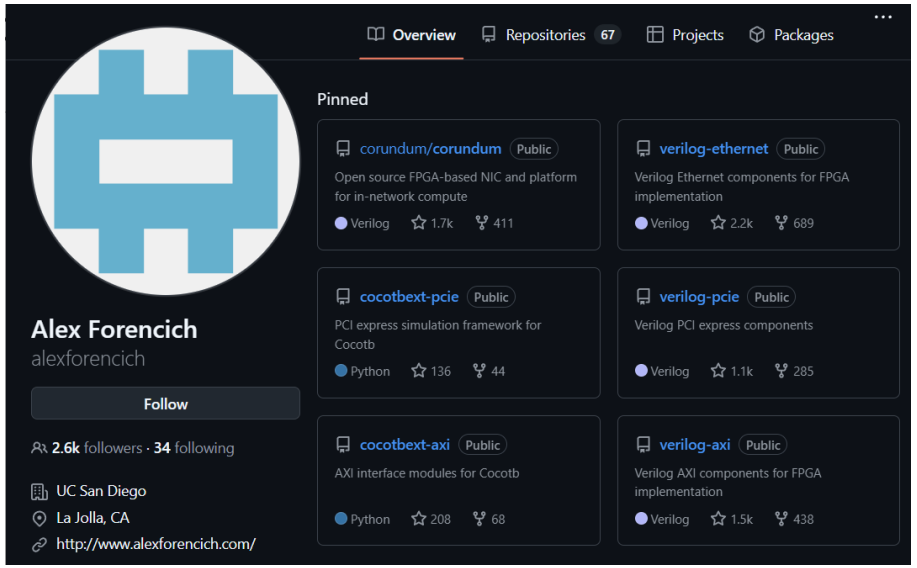
SKA (Square Kilometre Array) международный проект по созданию крупнейшего в мире радиоинтерферометра.



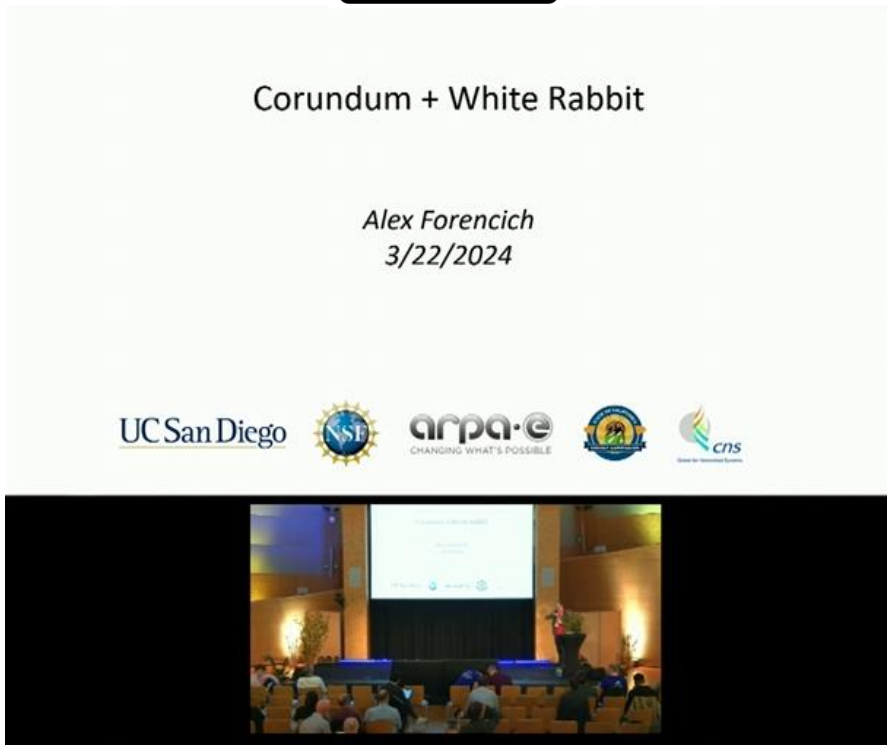
IceCube, нейтринная обсерватория на Южном полюсе, представляет собой детектор частиц объемом кубический километр, изготовленный из антарктического льда и расположенный недалеко от станции Амундсен-Скотт на Южном полюсе.

Alex Forencich, Corundum и Кролик

Corundum is an open-source, high-performance FPGA-based NIC and platform for in-network



SCAN ME



Therefore, I am planning a rewrite of the works (corundum and all of the verilog libraries) in System Verilog under the CERN OHL strict license (similar to GPL) + a CLA, with an option for a paid commercial license.

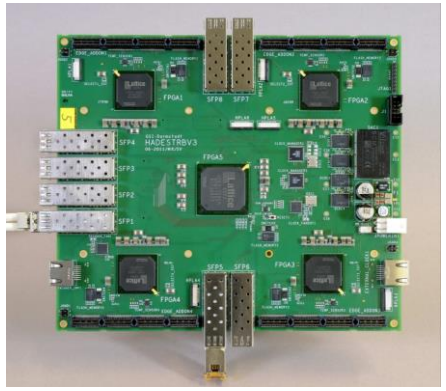
TRB3 – TDC

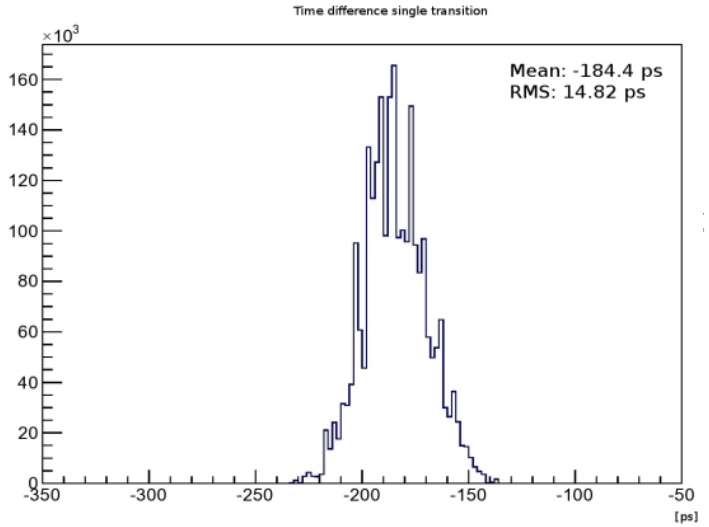
Существует с 2011 года

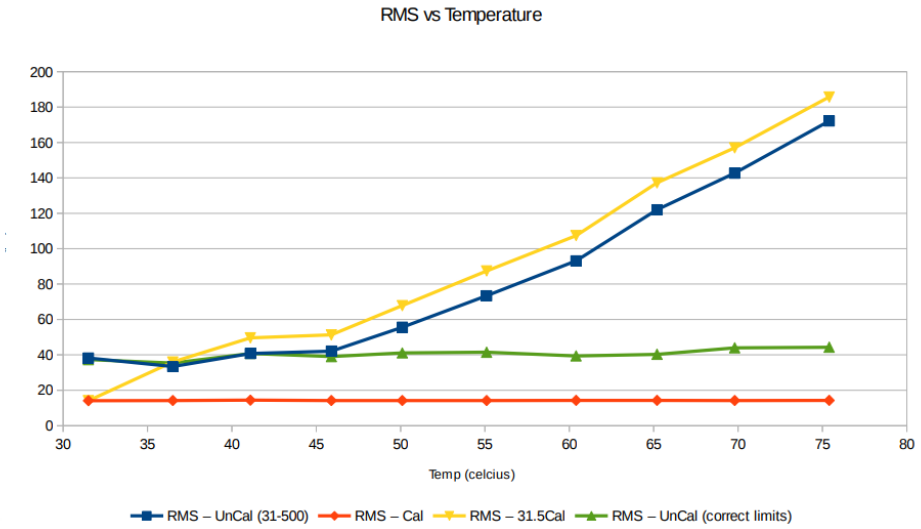
GSI Helmholtzzentrum für Schwerionenforschung GmbH

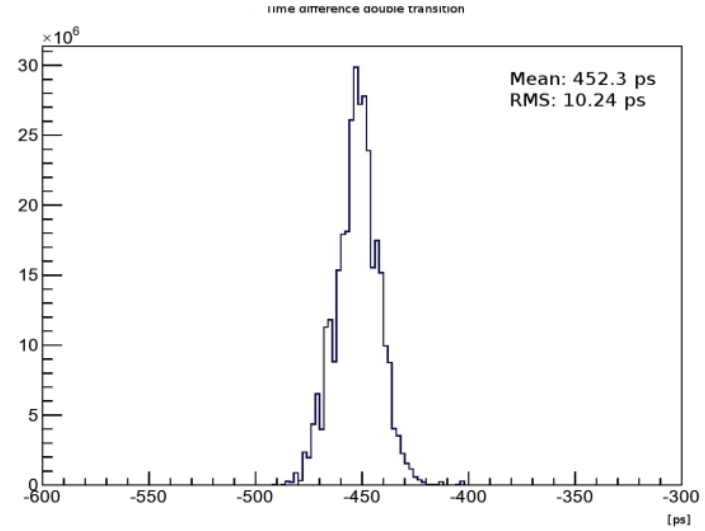
SCAN ME

- Проект GSI
- Точность < 20 ps
- Max Hit Rate 50 MHz
- Очень подробная документация
- Использовалось, в основном, для тестирования детекторов
- Доступны схемы всех ревизий и дополнительных модулей
- Доступны исходники* (Лицензия)









Time-to-Digital Converter IP-Core for FPGA at State of the Art

FABIO GARZETTI, (Member, IEEE), NICOLA CORNA, (Member, IEEE), NICOLA LUSARDI, (Member, IEEE), AND ANGELO GERACI, (Senior Member, IEEE)
Politecnico di Milano, 20133 Milano, Italy
Corresponding author: Fabio Garzetti (fabio.garzetti@polimi.it)

Implementation results and measurements. In particular, Artix-7 column refers to the device selected for testing the IP-Core.

Performance	Artix–7	Virtex–5	Spartan–6	Kintex–7	Zynq–7000	Kintex UltraScale
Resolution	366 fs	18 ps	25 ps	250 fs	2 ps	305 fs
Precision	8.0 ps r.m.s.	25.0 ps r.m.s.	17 ps r.m.s.	8.0 ps r.m.s.	12 ps r.m.s.	8.5 ps r.m.s.
Full Scale Range	10.3 s	10.7 s	640 ns	10.3 s	10.7 s	10.2 μs
DNL	250 fs	N.A.	N.A.	200 fs	1.4 ps	N.A.
INL	2.5 ps	N.A.	N.A.	2.2 ps	5 ps	N.A.
Number of Channels	16	16	4	16	8	24
Channel Rate	150 MHz	5 MHz	N.A.	150 MHz	45 MHz	50 MHz
Dead–Time	5 ns	N.A.	N.A.	5 ns	20 ns	N.A.
Temperature Sensitivity	286 fs/°C	N.A.	N.A.	N.A.	N.A.	N.A.

HLS4ML, Conifer, fwX

HLS4ML – 35 человек / 13 организаций

Conifer – 13 человек

fwX – 5 человек (+ 13)

Backend

HLS4ML (Универсальный)

- Vivado HLS
- Intel HLS

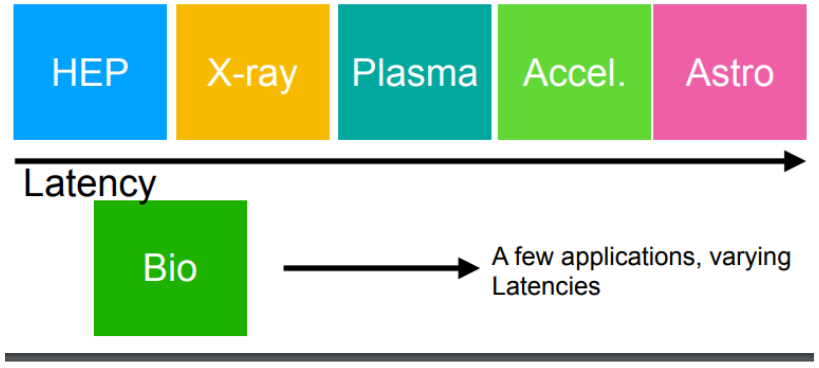
Conifer (Оптимизированный)

- Vivado/Vitis HLS
- VHDL

fwX (Для профильной задачи)

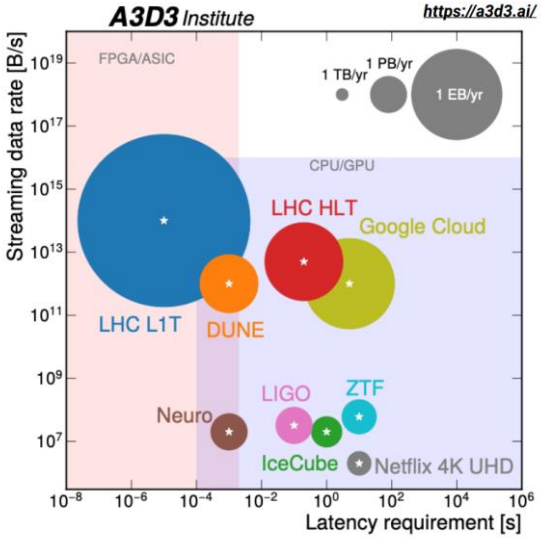
- Vivado HLS

When an Software Engineer asks you why FPGAs are "hard to program":



FAST ML

- Beam control
- ML for compression
- ML for tracking
- ML for reconstruction



	GPU Tesla V100	FPGA XCV13P with hls4ml
Latency	5 ms	~350 ns

Model (quantized/pruned)

Quantized:

QONNX

QKERAS

Convert model to internal representation

Write HLS project targeting specified backend

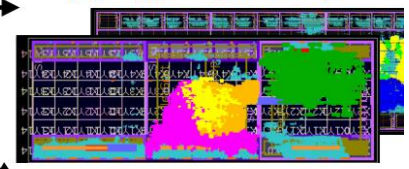
Run emulation

Run synthesis

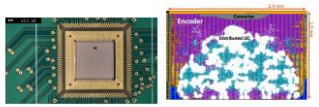
Vivado/Vitis best supported
Intel Quartus
Intel One API
Mentor Catapult HLS
available soon

Co-processing kernel (Xilinx accelerators/SoCs)

FPGA custom designs (eg trigger algorithms)



ASICs



Аппаратные фильтры данных

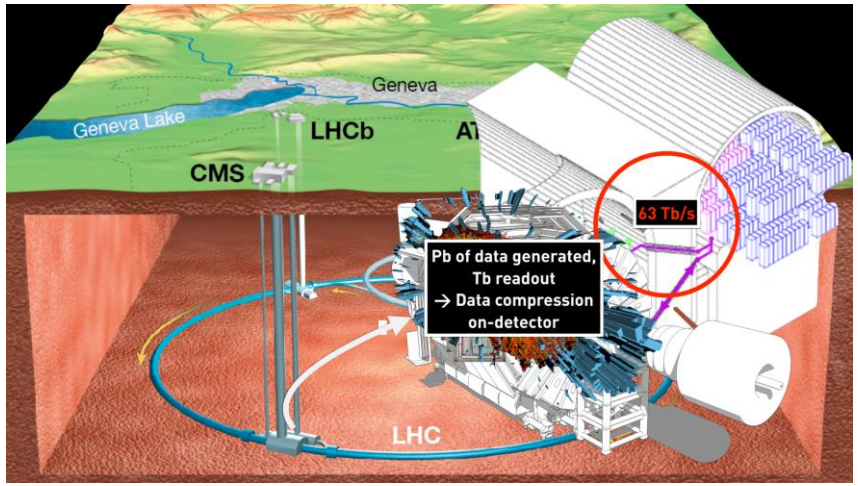
Сейчас

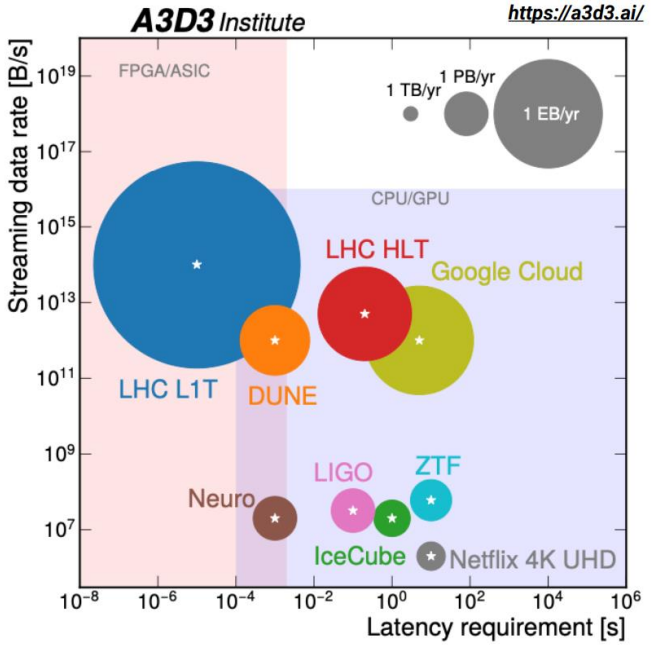
“Particles collide in the Large Hadron Collider (LHC) detectors approximately 1 billion times per second, generating about one petabyte of collision data per second.”

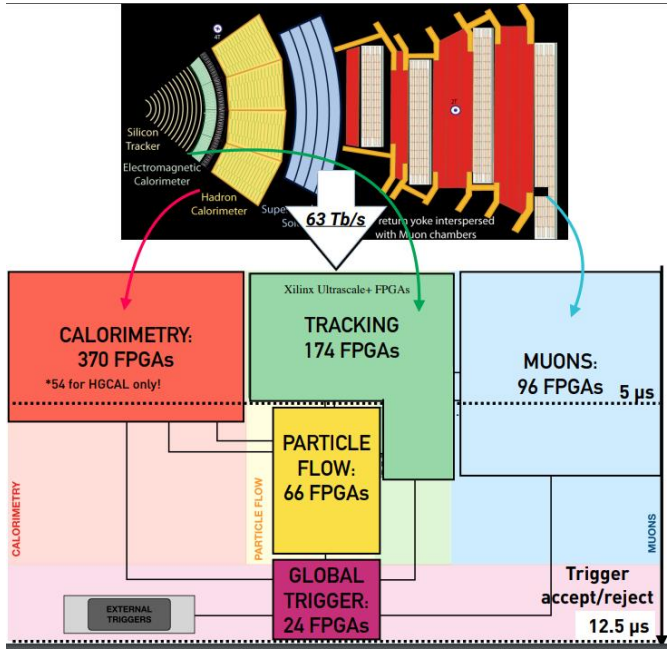
Планируется

High Luminosity LHC (2030)

- *x10 data size*
- *x3 collisions/s*







Pixel Detector + eFPGA + ML

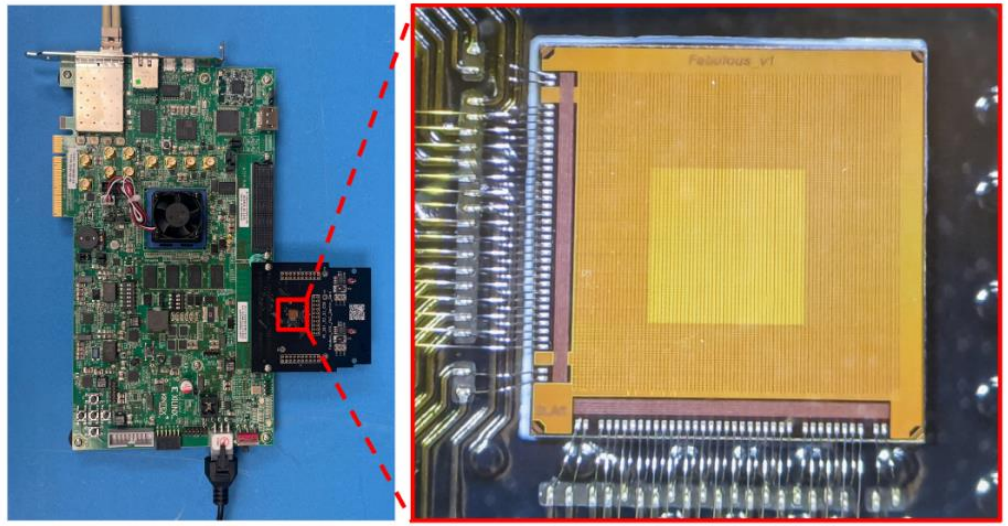
Conifer

- Filter pT > 2 GeV
- 28 nm eFPGA
- 25 ns latency
- 500 LUTs

В будущем, позволит ощутимо уменьшить поток данных с детекторов за счет отбора событий.

Принцип применим и к другим типам детекторов.

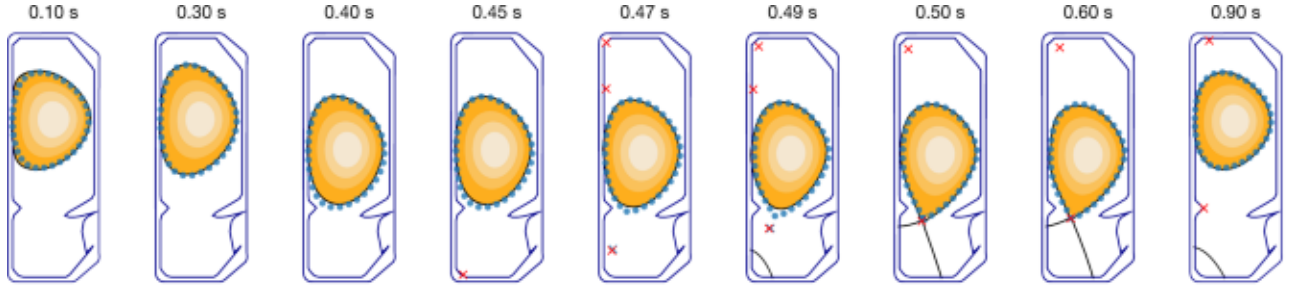
SCAN ME



Signal Efficiency	Background Rejection	Classification threshold
96.4%	5.8%	0.4953
97.8%	3.9%	0.4922

TOKAMAK stabilization

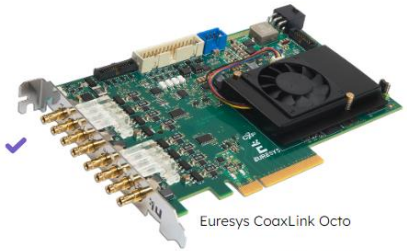
Tokamak —установка для магнитного удержания плазмы с целью достижения условий, необходимых для протекания управляемого термоядерного синтеза.

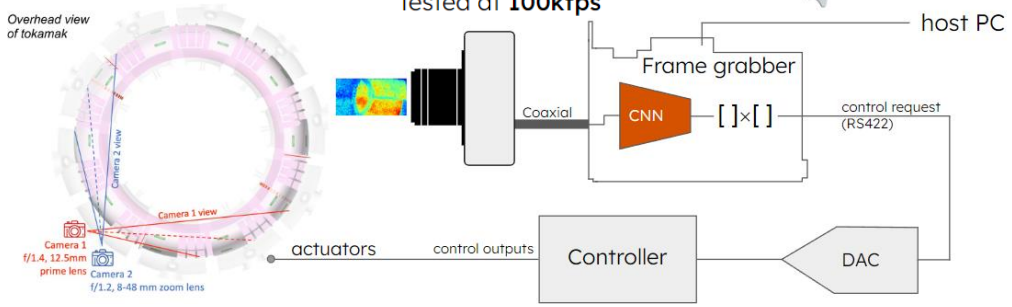


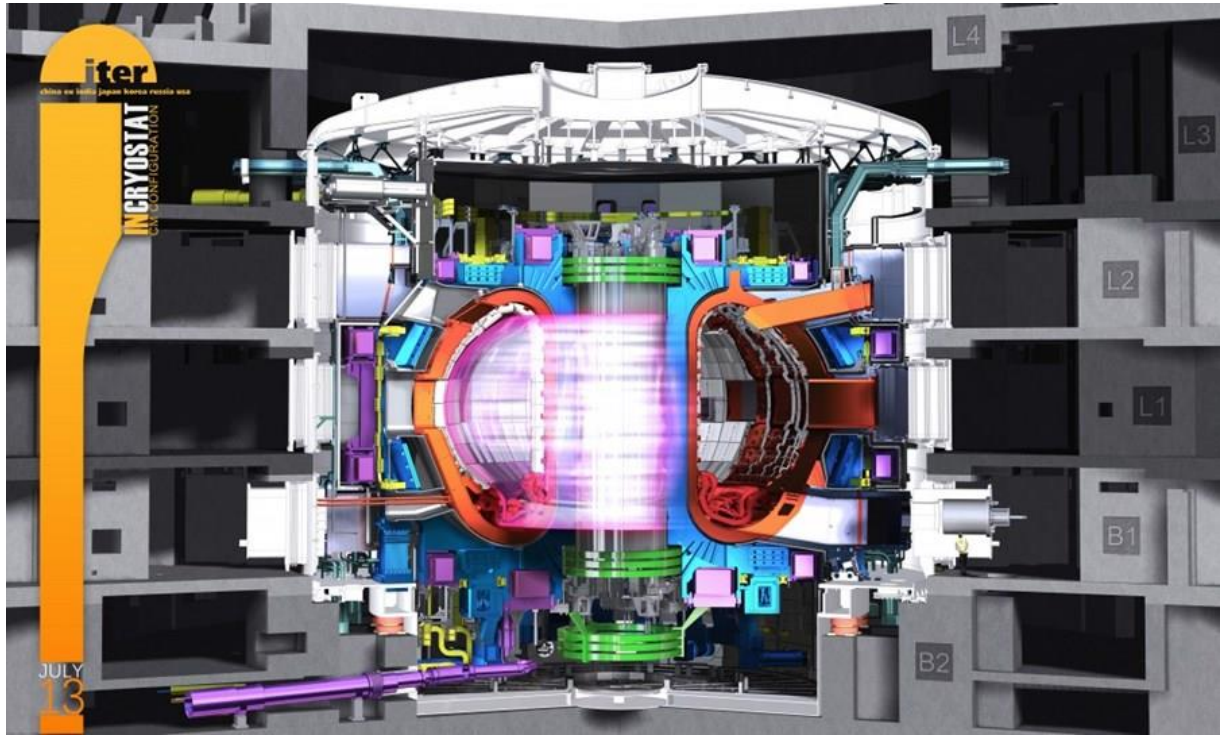
Hardware deployment

- Wait... many frame grabbers are FPGA-based!
  - Inference latency satisfactory (<20us) ✔
  - Deterministic timing ✔
  - **Zero PCIe hops, all computation done on-chip** ✔
  - Highly power efficient ✔

Model Latency: 7.7us
Full latency: 17.6us
Tested at **100kfps**

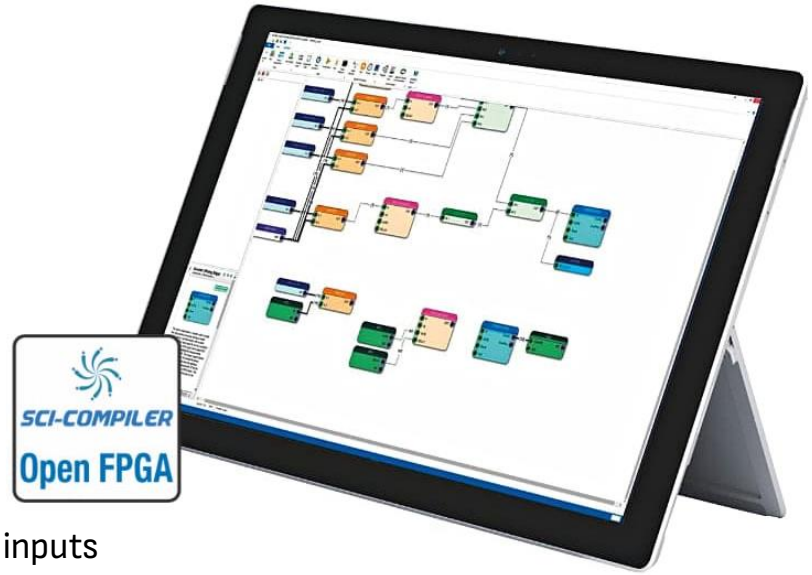




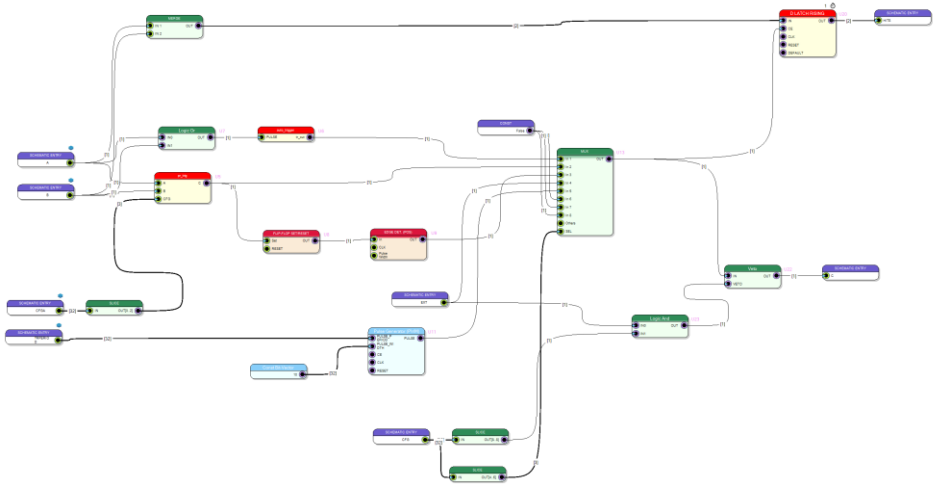


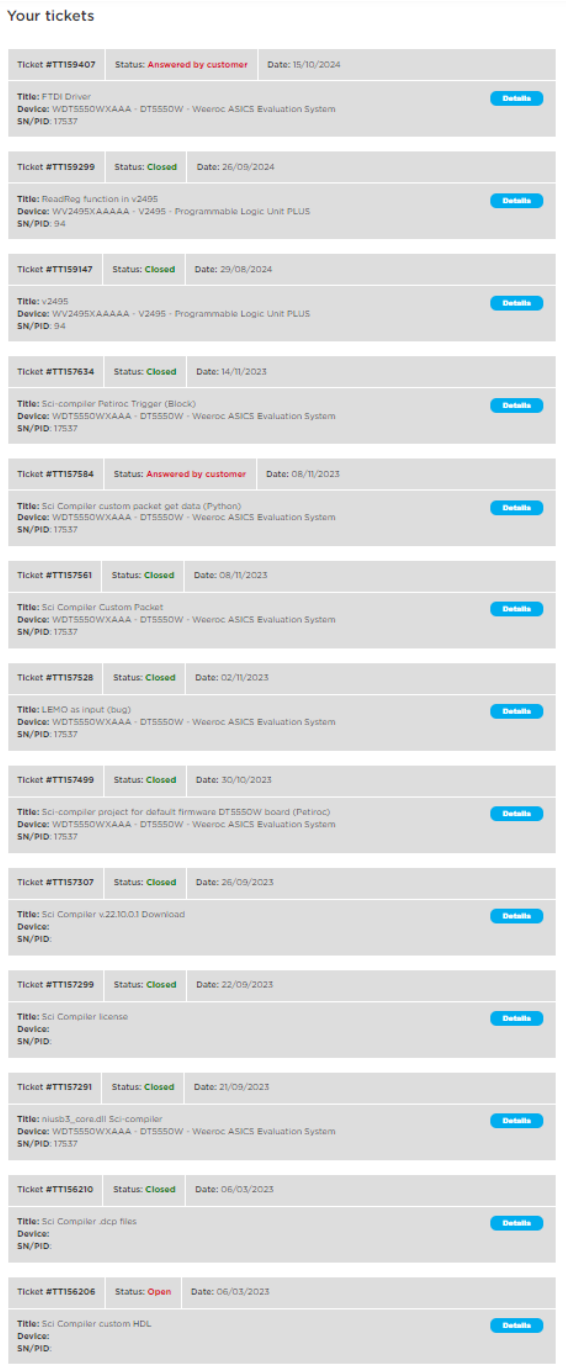
CAEN

- Open FPGA (Sci-compiler)



- DT5495 – V2495 Programmable Logic Units
- DT5550 DAQ System with User Programmable FPGA and sequencer
- DT5550W Weeroc ASICs Development system
- R5560 128-channel Open FPGA Digitizer with differential inputs
- R5560SE 128-channel Open FPGA Digitizer with single-ended inputs
- DT5560SE 32-channel Open FPGA Digitizer
- 2740–2745 Digitizer Families





Еще больше OpenSource

HDL MODULES

website hdl-modules.com | github hdl-modules/hdl-modules | license BSD 3-Clause
chat GitHub Discussions | ci passing

The hdl-modules project is a collection of reusable, high-quality, peer-reviewed VHDL building blocks. It is released as open-source project under the very permissive BSD 3-Clause License.

This website contains human-readable documentation of the modules. To check out the source code, go to the GitHub page.

The code is designed to be reusable and portable, while having a clean and intuitive interface. Resource utilization is always critical in FPGA projects, so these modules are written to be as efficient as possible. Using generics to enable/disable different features and modes means that resources can be saved when not all features are used. Some entities are very deliberately area optimized, such as the FIFOs, since they are used very frequently in FPGA projects.

More important than anything, however, is the quality. Everything in this project is peer reviewed, has good unit test coverage, and is proven in use in real FPGA designs. All the code is written with readability and maintainability in mind.

The following things can be found, at a glance, in the different modules:

- axi: AXI3/AXI4 Crossbars, FIFOs, CDCs, etc.
- axi_lite: AXI-Lite Crossbars, FIFOs, CDCs, etc.
- bfm: Many BFMs for simulating AXI/AXI-Lite/AXI-Stream.
- common: Miscellaneous, but useful, things that do not fit anywhere else.
- fifo: Synchronous and asynchronous FIFOs with AXI-stream-like handshake interface.
- hard_fifo: Wrappers, with cleaner AXI-stream-like handshake interfaces, around hard FIFO primitives.
- lfsr: Maximum-length linear feedback shift registers for pseudo-random number generation.
- math: Some common math function implementations.
- reg_file: A generic register file and a simulation support package for register operations.
- resync: CDC implementations for different signals and buses, along with proper constraints.
- sine_generator: Professional sinusoid waveform generator (or DDS, NCO).

На данный момент ограничен доступ

colibri

Open Source, Vendor Independent VHDL Common Library

This library is a collection of common components, functions, and procedures used in CERN gateware projects. The scope of the library is to simplify and standardise the development of gatewares for CERN.

Structure

- colibri.common Common Functions
- colibri.pipes Pipes entities (Arbiter, Router, ...)
- colibri.fileio File Operations
- colibri.memory Memory Entities (FIFOs, RAMs)
- colibri.comms Utilities for Communications (scrambler, PRBS, ...)
- colibri.interfaces Bus and Stream Protocols Components (AXI, Avalon, Wishbone, ...)
- colibri.io Input Output protocols (UART, I2C, ...)
- colibri.misc Miscellaneous

Everything in this repository should be compiled under `colibri` library.

Testbenches are available in the sim directory, formal verification tests are available in the fv directory.

License

The content of this repository is licensed under CERN-OHL-W-v2.

How to contribute

Contributing in the form of code, feedback, ideas or bug reports are welcome. Code contributions are expected to have self-checking testbenches, formal verification tests, and pass the style checks. If there are any problems let us know.

Before doing any major changes we recommend creating an issue or chatting with us on mattermost to discuss first. In this way you do not get started on the wrong track and waste time.

Contributors

2023 - 2024 @alperro alberto.perro (at) cern.ch
2024 @mvodnik mitja.vodnik (at) cern.ch

FDF 2024

SCAN ME

- Sharable HDL Cores
- Solutions to everyday digital design problems
- Algorithm implementation
- HDL development, verification, and simulation tools

High-Level Synthesis for Machine Learning — Nicolo Ghielmetti
30/7-018 - Kjell Johnsen Auditorium, CERN 16:15 - 16:45

Under the Canopy: Exploring Conifer for Low-Latency Decision Forests on FPGAs — Sioni Paris Summers
30/7-018 - Kjell Johnsen Auditorium, CERN 16:45 - 17:15

UVVM – An introduction to the world's fastest growing FPGA verification methodology — Espen Tallaksen
30/7-018 - Kjell Johnsen Auditorium, CERN 17:15 - 17:55

LoCod: an open-source hardware/software co-design tool for SoC/FPGA — Fiorent Manni
30/7-018 - Kjell Johnsen Auditorium, CERN 17:55 - 18:15

16:00
Convenient and reliable clock domain crossings, using scoped constraints and reusable blocks — Lukas Vik
30/7-018 - Kjell Johnsen Auditorium, CERN 15:40 - 16:20

COLIBRI: Towards a CERN-wide common cores library — Alberto Perro
30/7-018 - Kjell Johnsen Auditorium, CERN 16:20 - 16:50

17:00
CERN control group cores and tools — Tristan Gingold
30/7-018 - Kjell Johnsen Auditorium, CERN 16:50 - 17:20

Fast Monitoring of FPGA algorithms using SpyBuffers — Iacopo Longarini
30/7-018 - Kjell Johnsen Auditorium, CERN 17:20 - 17:50

18:00
The BondMachine Project — Mirko Mariotti et al.
30/7-018 - Kjell Johnsen Auditorium, CERN 17:50 - 18:20

09:00
YML2HDL tool — Thiago Costa De Paiva
30/7-018 - Kjell Johnsen Auditorium, CERN 09:00 - 09:20

Automatic code generation for managing the firmware and software for configuration/status registers and memories in — Anna Malgorzata Kulinska

Assertion-Based Formal Debugging During RTL Development — N. Engelhardt

10:00
30/7-018 - Kjell Johnsen Auditorium, CERN 09:40 - 10:15

Open source formal verification with SymbiYosis — Yann Thoma
30/7-018 - Kjell Johnsen Auditorium, CERN 10:15 - 10:45

Coffee Break
30/7-018 - Kjell Johnsen Auditorium, CERN 10:45 - 11:15

11:00
Becoming vendor agnostic with the help of model-based source code generation — Alexander Wirthmüller
30/7-018 - Kjell Johnsen Auditorium, CERN 11:15 - 11:50

HDL on git (Hog) — Nordin Aranzabal Barrio
30/7-018 - Kjell Johnsen Auditorium, CERN 11:50 - 12:20

12:00
Summary of 1st FDF meeting — Dr Rui Zou
30/7-018 - Kjell Johnsen Auditorium, CERN 12:20 - 12:40

Closing Remarks — Dr Francesco Gonnella
30/7-018 - Kjell Johnsen Auditorium, CERN 12:40 - 12:50

Fast Machine Learning for Science (Workshop)

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Спасибо за Внимание