

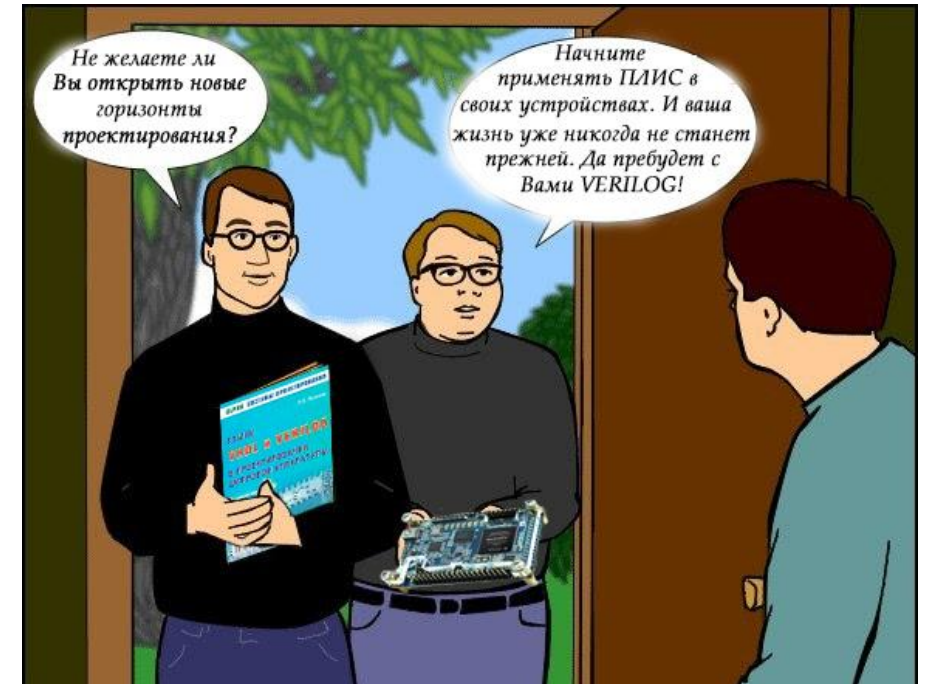
# Плюсы, Наука, Зачем?

## *Или жизнь FPGA в научной среде*

Александр Бойков

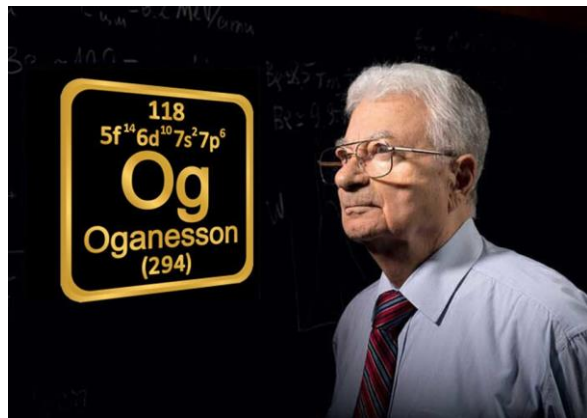
# Дисклеймер

- Материал скорее популярный, чем технический
- Мнение автора может не совпадать с мнением коллег
- Тут нет UVM, CoSoTB и.т.д.
- Впереди 17 слайдов
- Много распространяется под лицензиями CERN OHL-(P/W/S)
- Ссылки на источники будут за QR-кодами

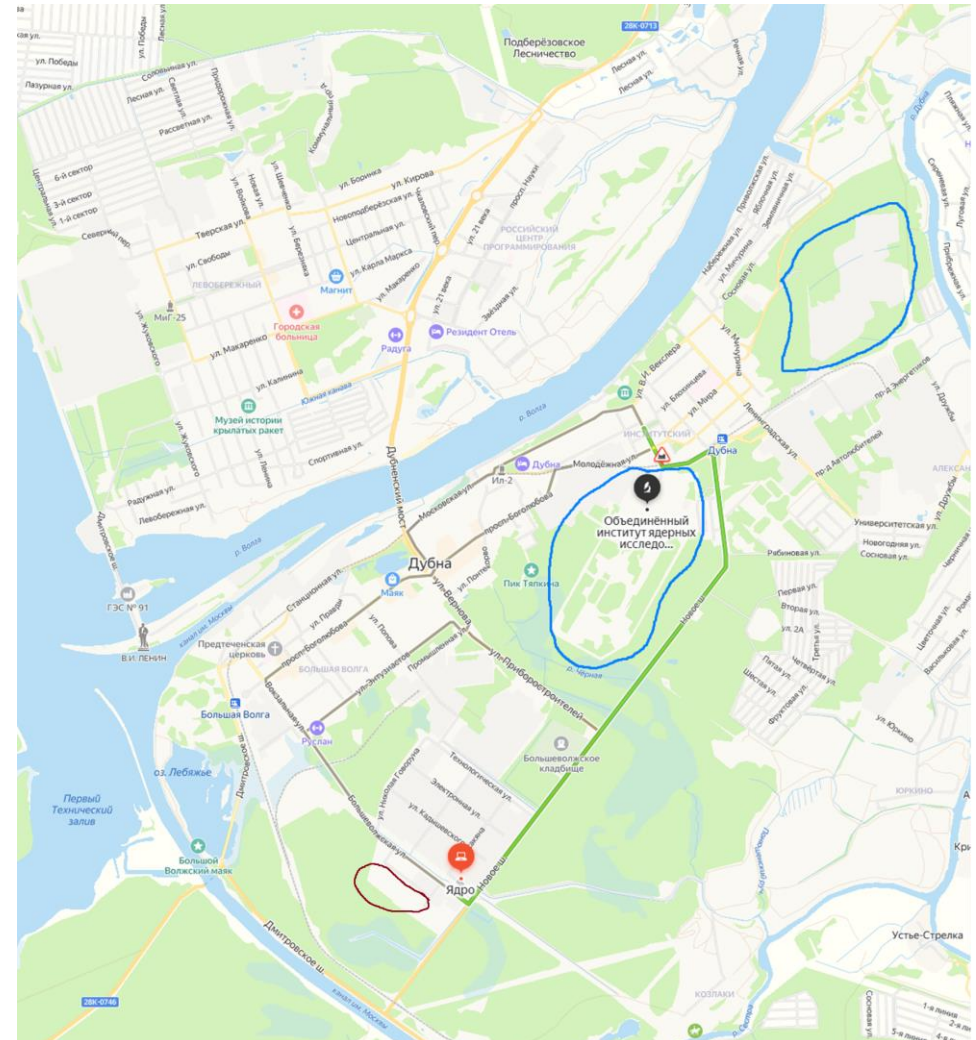


# ОИЯИ/JINR

Объединенный институт ядерных исследований — международная межправительственная научно-исследовательская организация, созданная на основе Соглашения, подписанного одиннадцатью странами-учредителями 26 марта 1956 г.

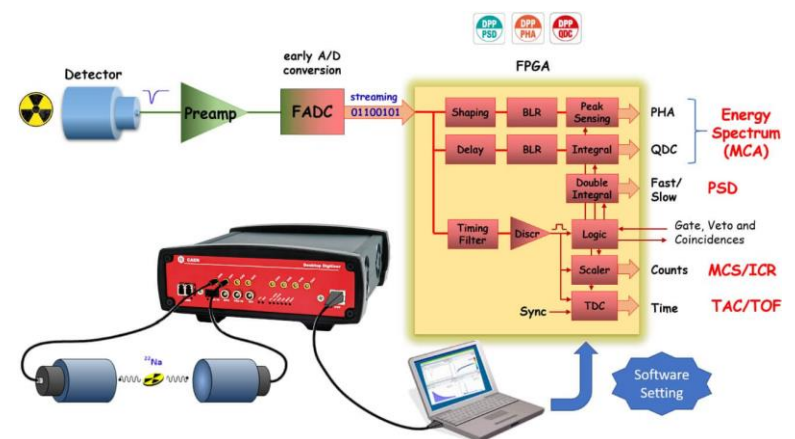
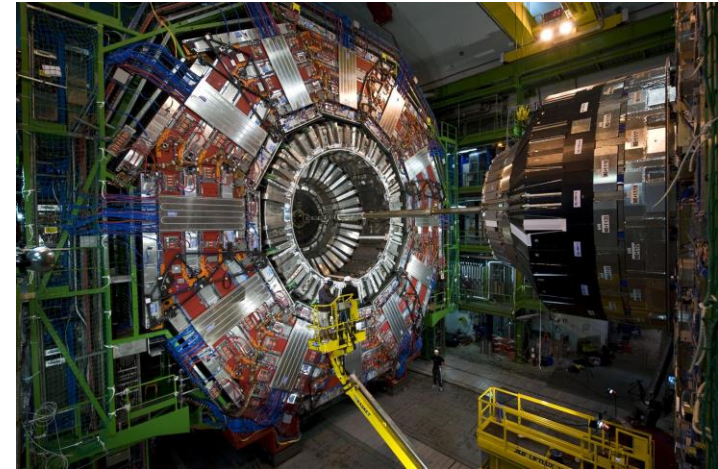
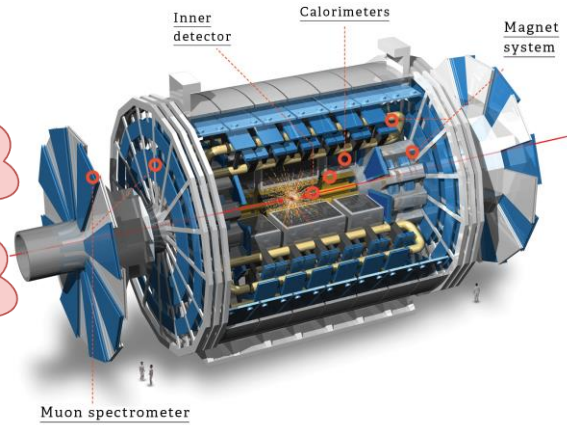
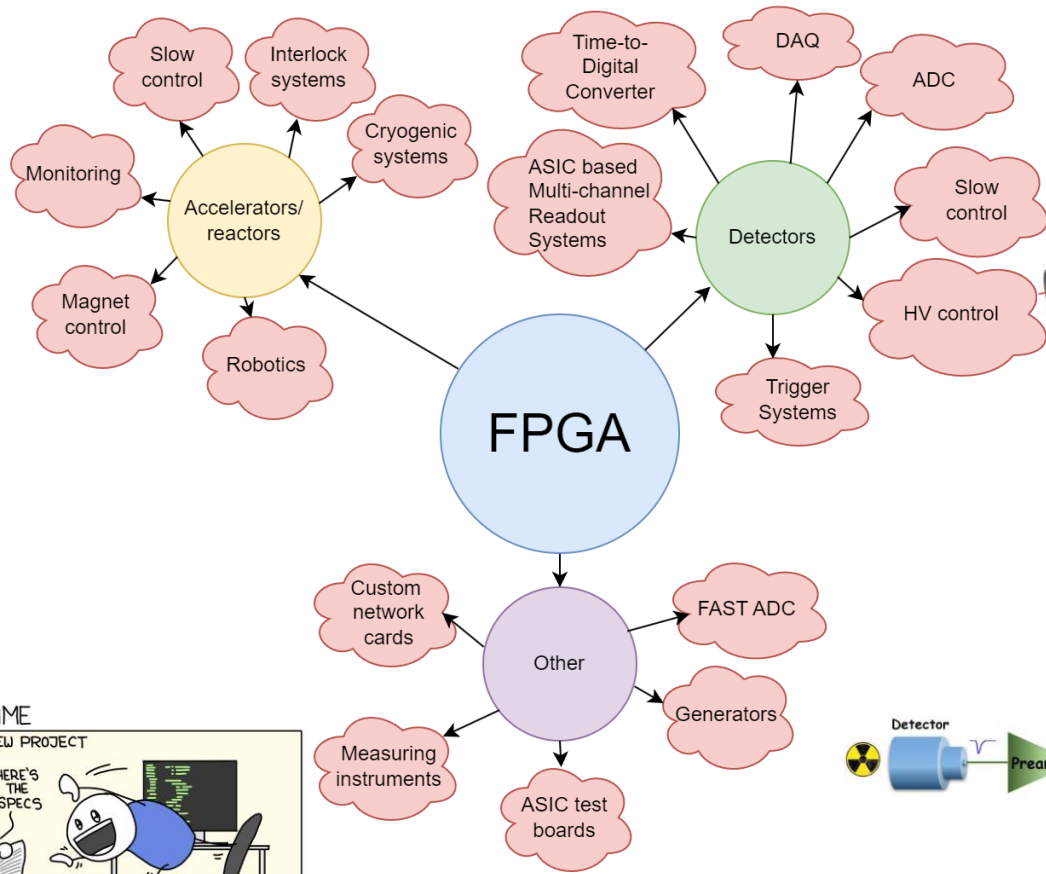


В ОИЯИ синтезировали элементы завершающие седьмой период таблицы Менделеева: 114 (флеровий), 115 (московий), 116 (ливерморий), 117 (теннессин) и 118 (оганесон)





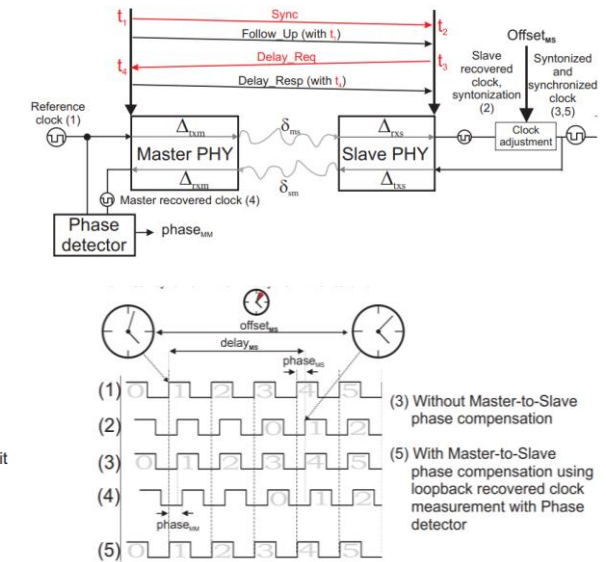
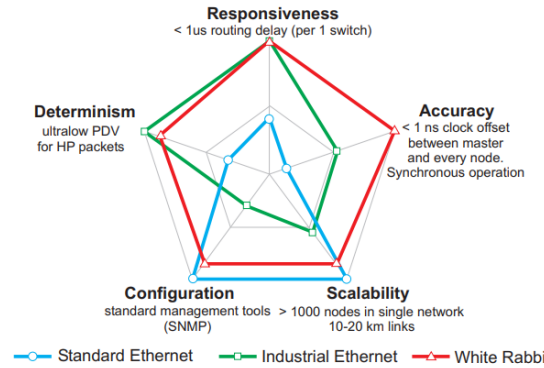
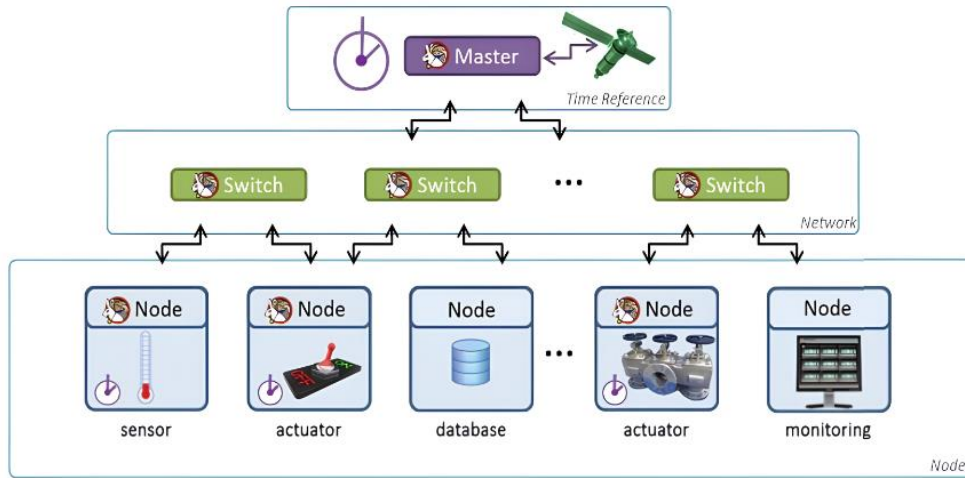
# Мейнструм



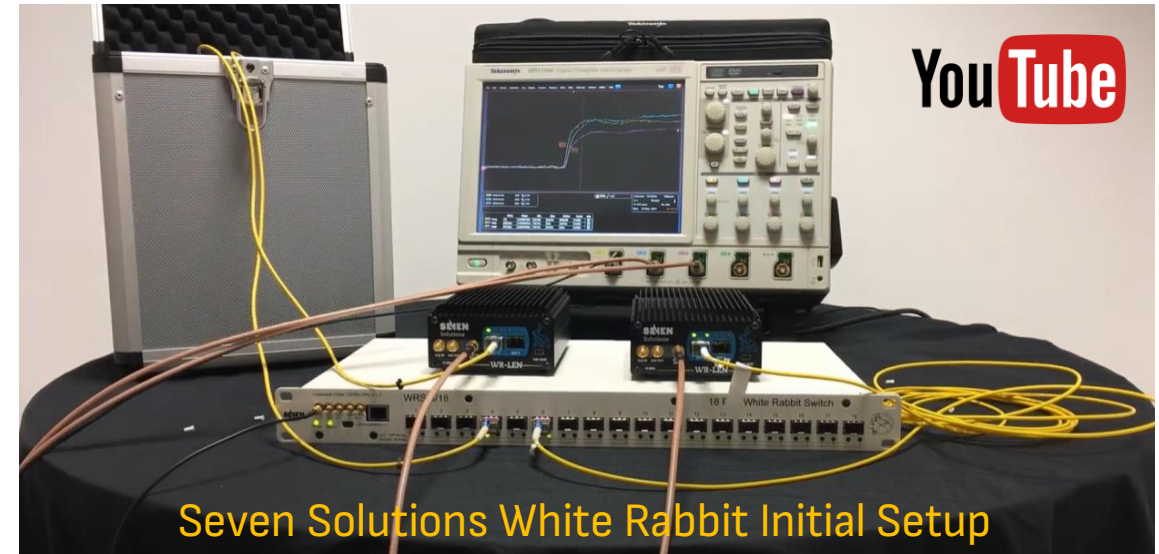
# Кролик



The White Rabbit Project



- Синхронизация с точностью 1 Нс или лучше
- Стабильно поддерживает сети с длиной связи до 10 Км (VTT MIKES успешно достиг 1000км с точностью 50нс)
- *Потенциально* нет ограничений в размере сети
- Доступны исходники IP и документация (лицензия)
- Поднимали на Virtex-6, Artix-7, UltraScale+... (более 10 платформ)





# Кролик. Зачем?



Физика высоких энергий



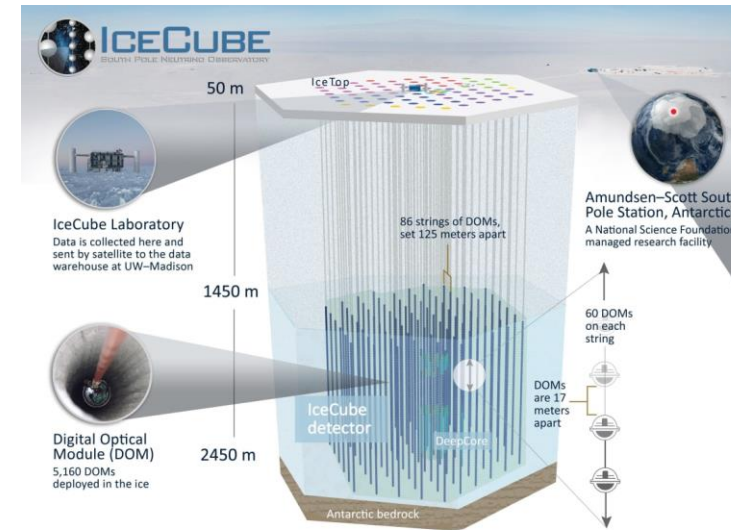
NICA (Nuclotron based Ion Collider Facility), JINR, Russia



LHC (Large Hadron Collider), CERN, Switzerland

Астрономия (телескопы)

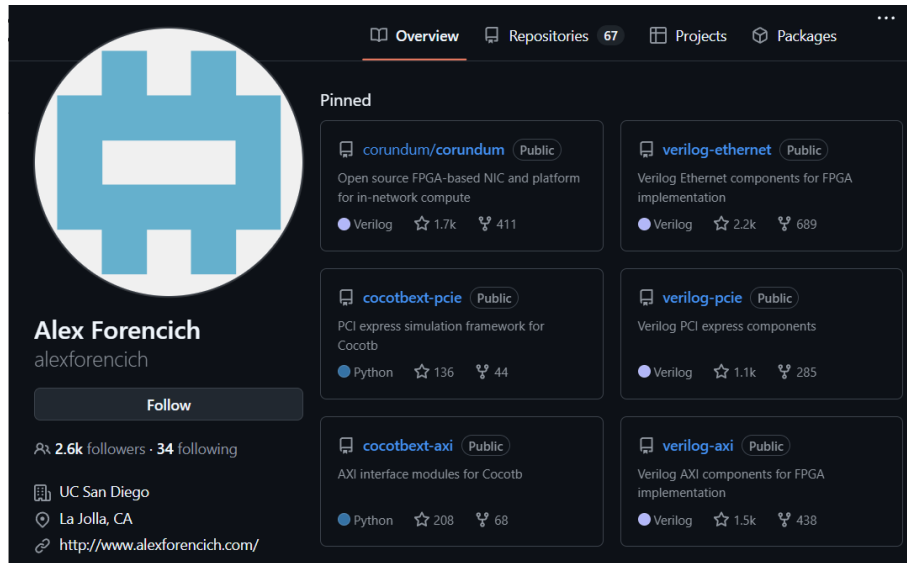
SKA (Square Kilometre Array) международный проект по созданию крупнейшего в мире радиointерферометра.



IceCube, нейтринная обсерватория на Южном полюсе, представляет собой детектор частиц объемом кубический километр, изготовленный из антарктического льда и расположенный недалеко от станции Амундсен-Скотт на Южном полюсе.

# Alex Forencich, Corundum и Кролик

Corundum is an open-source, high-performance FPGA-based NIC and platform for in-network



A screenshot of Alex Forencich's GitHub profile. The profile includes a blue and white logo, the name "Alex Forencich" with the handle "alexforencich", and a "Follow" button. It shows 2.6k followers and 34 following. The location is listed as UC San Diego, La Jolla, CA, with the website "http://www.alexforencich.com/". The "Pinned" section displays six repositories:

- corundum/corundum** (Public): Open source FPGA-based NIC and platform for in-network compute. 1.7k stars, 411 forks.
- verilog-ethernet** (Public): Verilog Ethernet components for FPGA implementation. 2.2k stars, 689 forks.
- cocotbext-pcie** (Public): PCI express simulation framework for Cocotb. 136 stars, 44 forks.
- verilog-pcie** (Public): Verilog PCI express components. 1.1k stars, 285 forks.
- cocotbext-axi** (Public): AXI interface modules for Cocotb. 208 stars, 68 forks.
- verilog-axi** (Public): Verilog AXI components for FPGA implementation. 1.5k stars, 438 forks.



A presentation slide titled "Corundum + White Rabbit" by Alex Forencich, dated 3/22/2024. The slide features logos for UC San Diego, NSF, ARPA-E (with the tagline "CHANGING WHAT'S POSSIBLE"), and CNS (with the tagline "Center for Networked Systems"). Below the logos is a photograph of a presentation stage with an audience.

Therefore, I am planning a rewrite of the works (corundum and all of the verilog libraries) in System Verilog under the CERN OHL strict license (similar to GPL) + a CLA, with an option for a paid commercial license.



# TRB3 – TDC

Существует с 2011 года



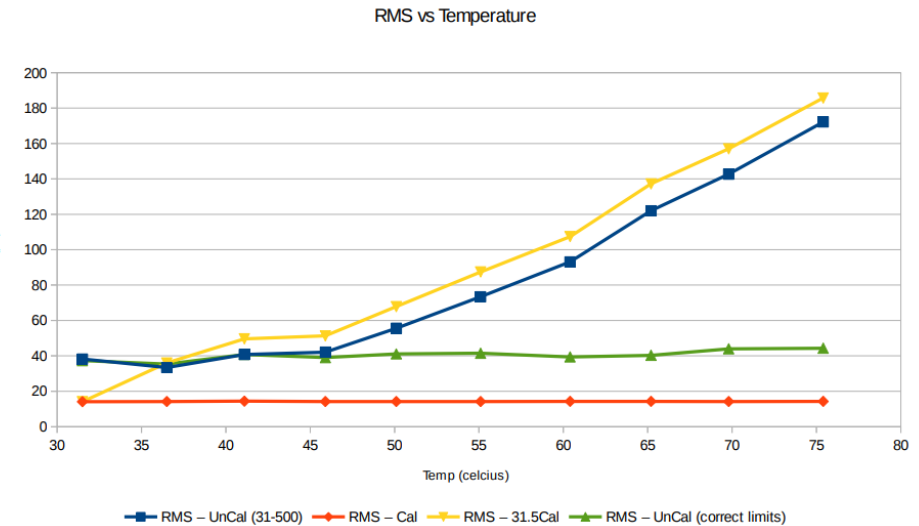
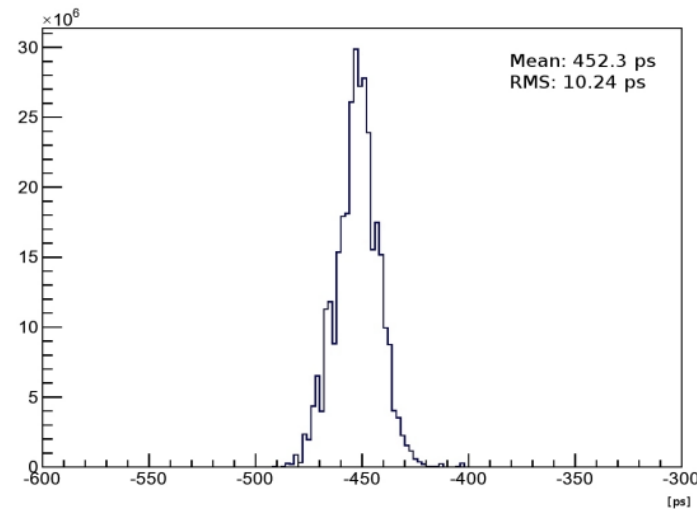
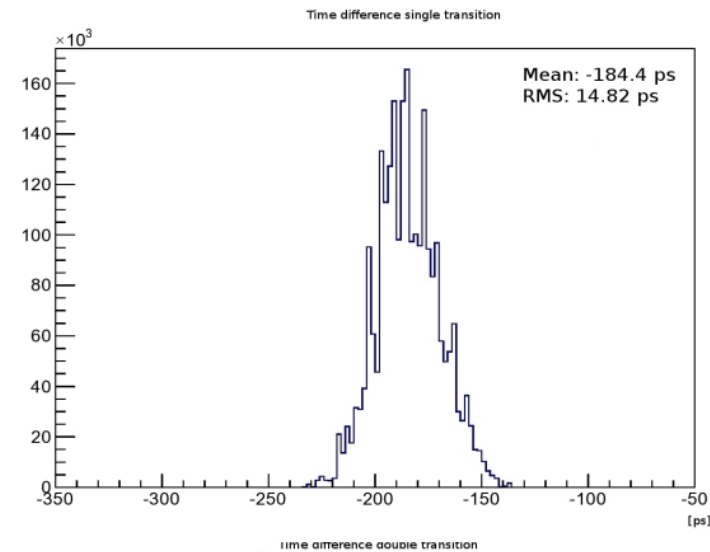
FAIR

GSI

GSI Helmholtzzentrum für Schwerionenforschung GmbH



- Проект GSI
- Точность < 20 ps
- Max Hit Rate 50 MHz
- Очень подробная документация
- Использовалось, в основном, для тестирования детекторов
- Доступны схемы всех ревизий и дополнительных модулей
- Доступны исходники\* (Лицензия)



## Time-to-Digital Converter IP-Core for FPGA at State of the Art

FABIO GARZETTI (Member, IEEE), NICOLA CORNA (Member, IEEE),  
NICOLA LUSARDI (Member, IEEE), AND ANGELO GERACI (Senior Member, IEEE)  
Politecnico di Milano, 20133 Milano, Italy  
Corresponding author: Fabio Garzetti (fabio.garzetti@polimi.it)

Implementation results and measurements. In particular, Artix-7 column refers to the device selected for testing the IP-Core.

Performance	Artix-7	Virtex-5	Spartan-6	Kintex-7	Zynq-7000	Kintex UltraScale
Resolution	366 fs	18 ps	25 ps	250 fs	2 ps	305 fs
Precision	8.0 ps r.m.s.	25.0 ps r.m.s.	17 ps r.m.s.	8.0 ps r.m.s.	12 ps r.m.s.	8.5 ps r.m.s.
Full Scale Range	10.3 s	10.7 s	640 ns	10.3 s	10.7 s	10.2 $\mu$ s
DNL	250 fs	N.A.	N.A.	200 fs	1.4 ps	N.A.
INL	2.5 ps	N.A.	N.A.	2.2 ps	5 ps	N.A.
Number of Channels	16	16	4	16	8	24
Channel Rate	150 MHz	5 MHz	N.A.	150 MHz	45 MHz	50 MHz
Dead-Time	5 ns	N.A.	N.A.	5 ns	20 ns	N.A.
Temperature Sensitivity	286 fs/ $^{\circ}$ C	N.A.	N.A.	N.A.	N.A.	N.A.



# HLS4ML, Conifer, fwX

HLS4ML – 35 человек / 13 организаций

Conifer – 13 человек

fwX – 5 человек (+ 13)

When an Software Engineer asks you why FPGAs are "hard to program":



Backend

HLS4ML (Универсальный)

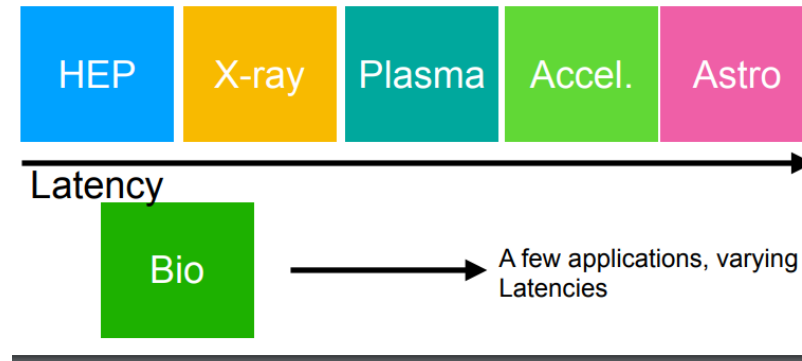
- Vivado HLS
- Intel HLS

Conifer (Оптимизированный)

- Vivado/Vitis HLS
- VHDL

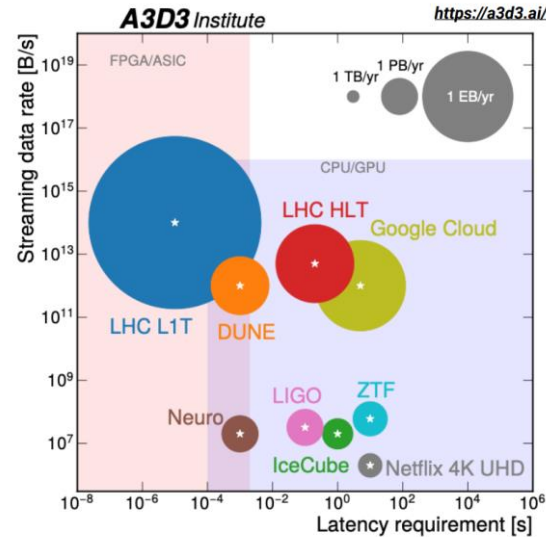
fwX (Для профильной задачи)

- Vivado HLS



# FAST ML

- Beam control
- ML for compression
- ML for tracking
- ML for reconstruction



	GPU Tesla V100	FPGA XCV13P with hls4ml
Latency	5 ms	~350 ns

Джон Коннор наблюдает как вы потихоньку заводите дружбу с нейросетями.



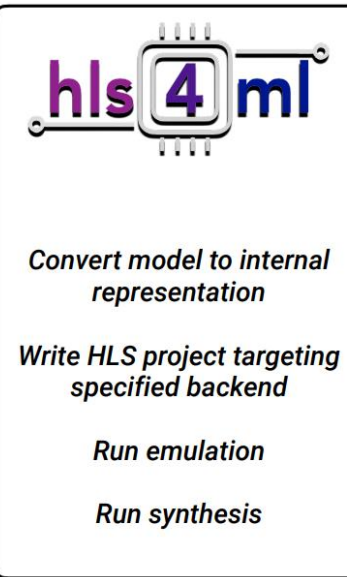
**PYTORCH**

Model  
(quantized/pruned)

Quantized:



QKERAS

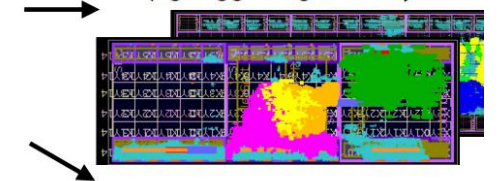


Vivado/Vitis best supported  
Intel Quartus  
Intel One API  
Mentor Catapult HLS  
available soon

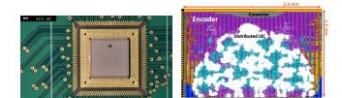


Co-processing kernel  
(Xilinx accelerators/SoCs)

FPGA custom designs  
(eg trigger algorithms)



ASICs



# Аппаратные фильтры данных

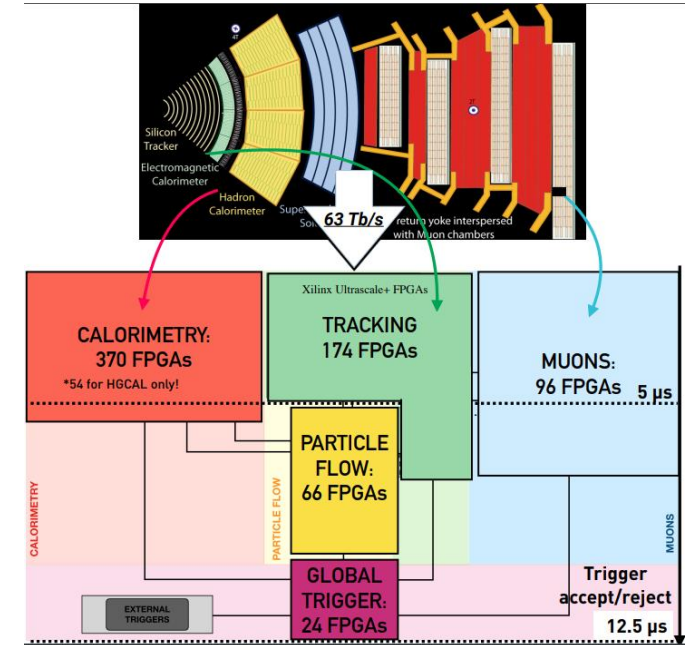
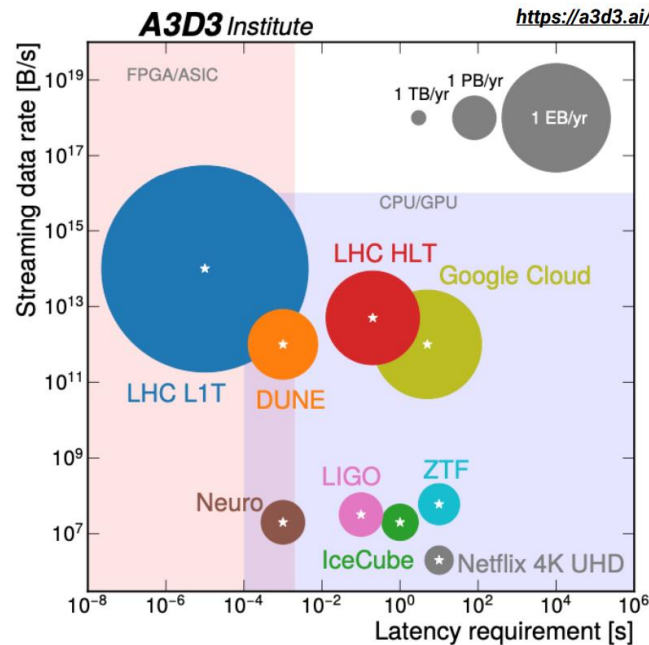
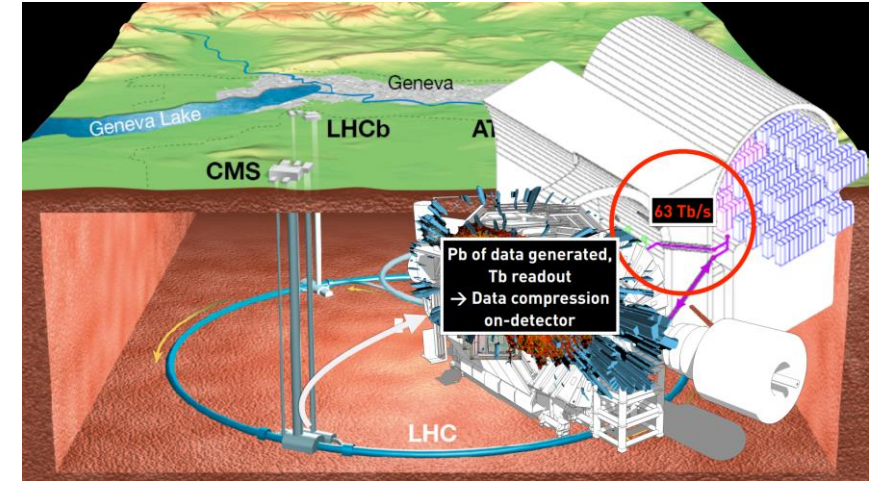
Сейчас

“Particles collide in the Large Hadron Collider (LHC) detectors approximately 1 billion times per second, generating about one petabyte of collision data per second.”

Планируется

*High Luminosity LHC (2030)*

- *x10 data size*
- *x3 collisions/s*



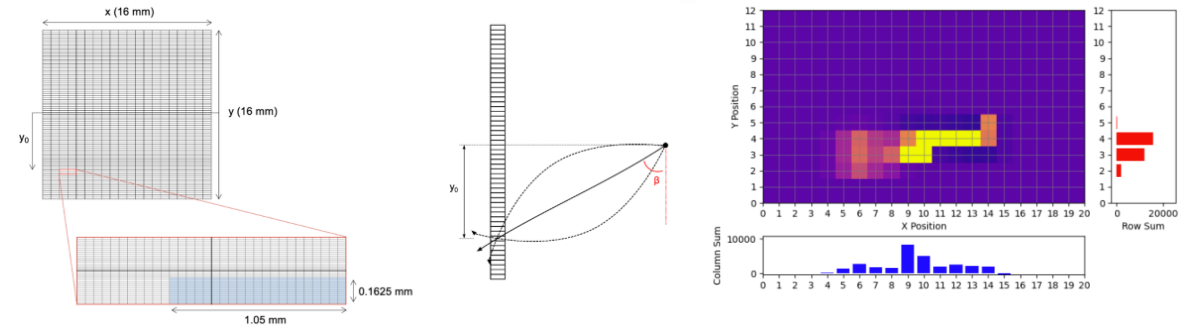
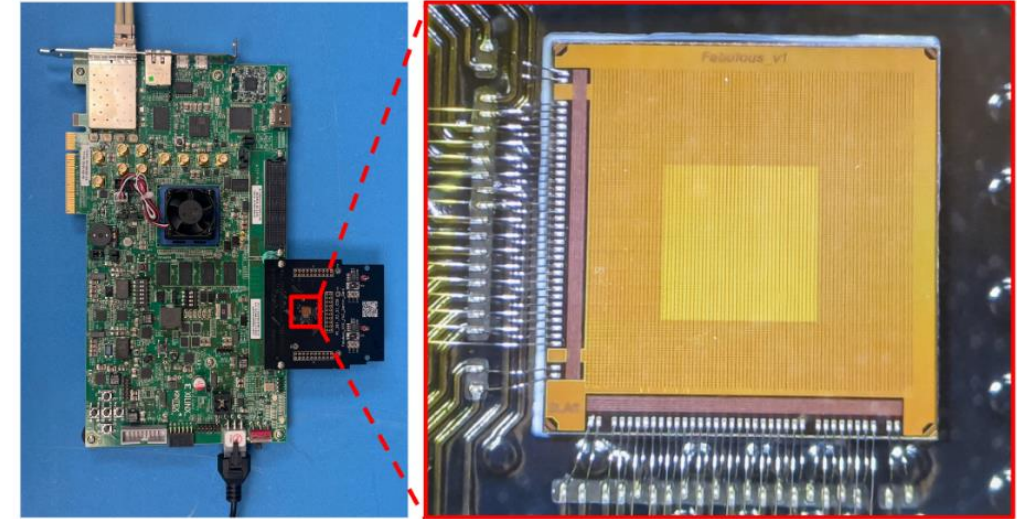


# Pixel Detector + eFPGA + ML

- Filter  $pT > 2$  GeV
- 28 nm eFPGA
- 25 ns latency
- 500 LUTs

В будущем, позволит  
ощутимо уменьшить поток  
данных с детекторов за  
счет отбора событий.

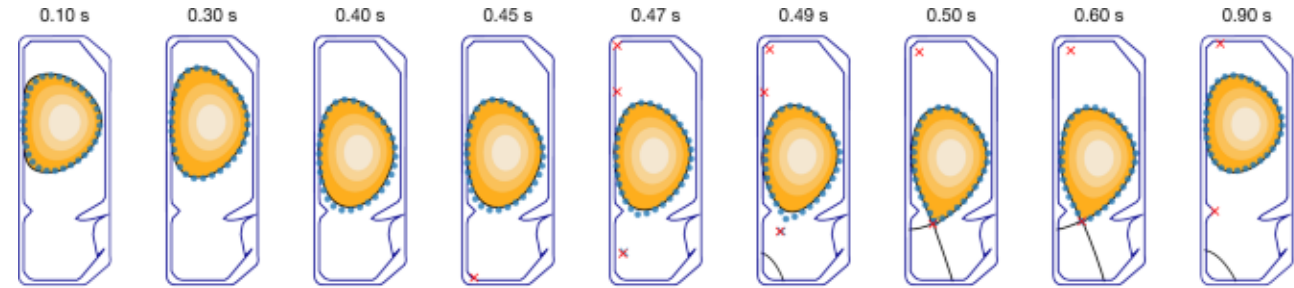
Принцип применим и к  
другим типам детекторов.



Signal Efficiency	Background Rejection	Classification threshold
96.4%	5.8%	0.4953
97.8%	3.9%	0.4922

# ТОКАМАК stabilization

Токамак — установка для магнитного удержания плазмы с целью достижения условий, необходимых для протекания управляемого термоядерного синтеза.



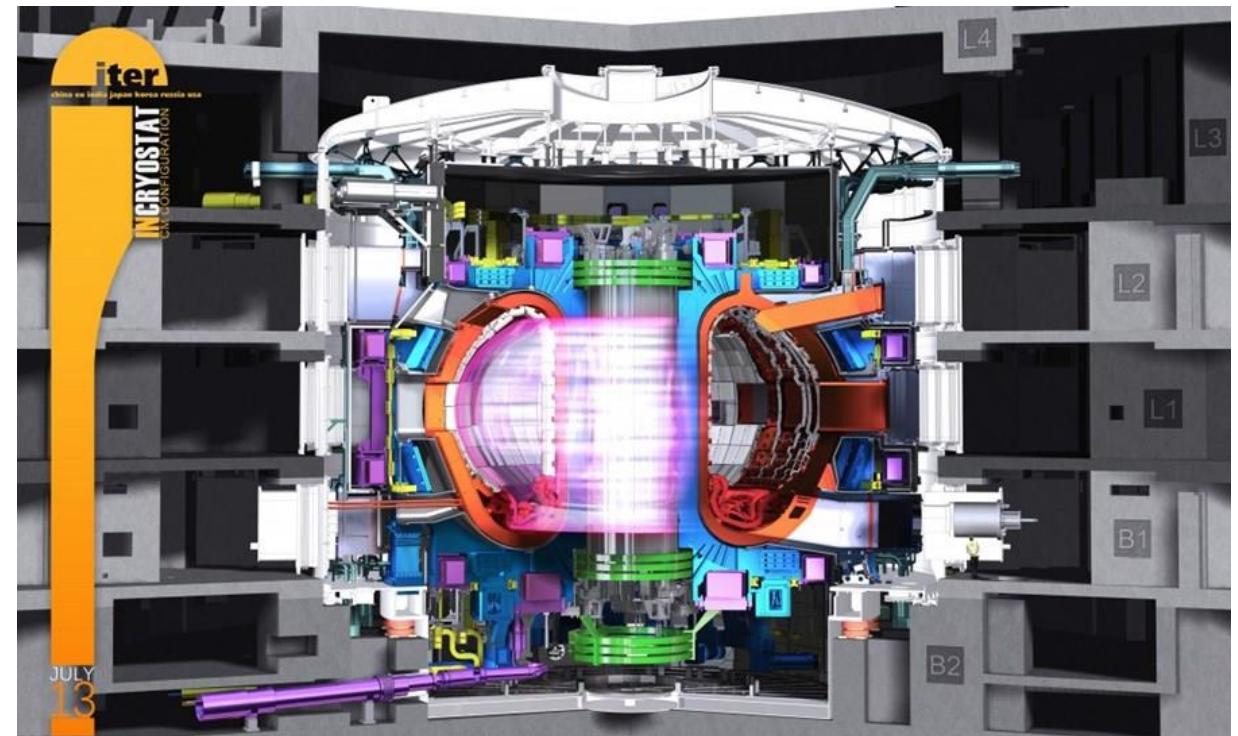
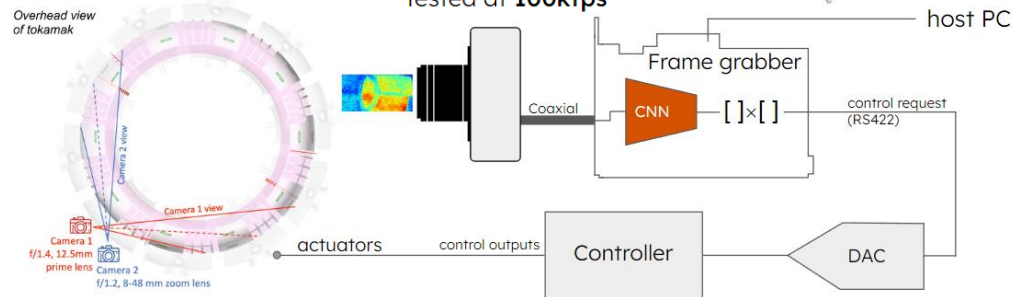
## Hardware deployment

- Wait... many frame grabbers are FPGA-based!
  - Inference latency satisfactory (<20us) ✓
  - Deterministic timing ✓
  - **Zero PCIe hops, all computation done on-chip** ✓
  - Highly power efficient ✓

**Model Latency: 7.7us**  
**Full latency: 17.6us**  
Tested at 100kfps



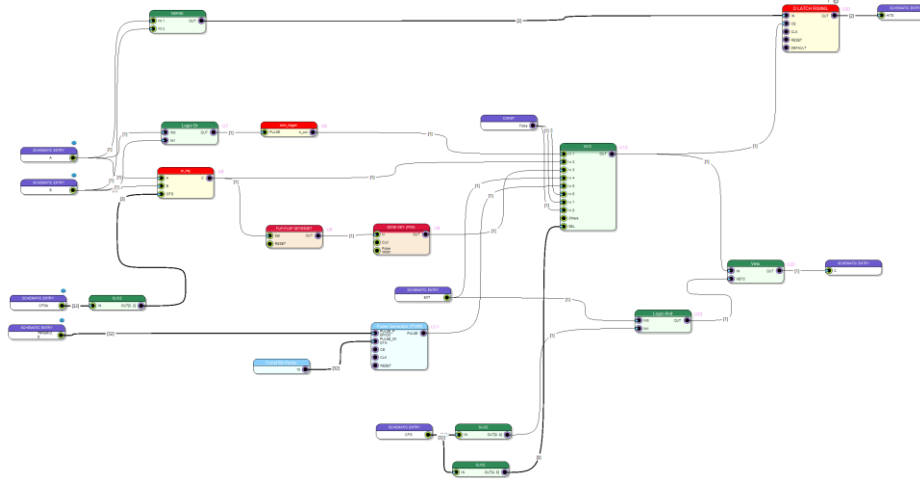
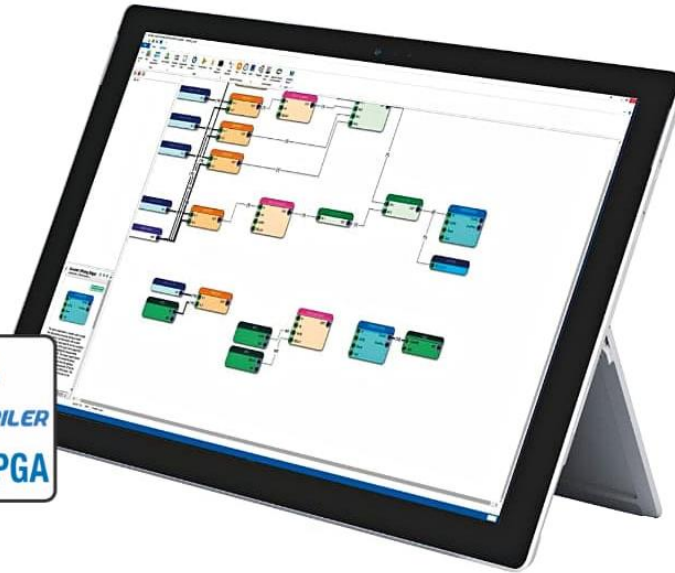
Euresys CoaxLink Octo



# CAEN

- Open FPGA (Sci-compiler)

- DT5495 – V2495 Programmable Logic Units
- DT5550 DAQ System with User Programmable FPGA and sequencer
- DT5550W Weeroc ASICs Development system
- R5560 128-channel Open FPGA Digitizer with differential inputs
- R5560SE 128-channel Open FPGA Digitizer with single-ended inputs
- DT5560SE 32-channel Open FPGA Digitizer
- 2740–2745 Digitizer Families



## Your tickets

Ticket #TT159407	Status: Answered by customer	Date: 15/10/2024	
Title: FTDI Driver Device: WDT5550WXXXX - DT5550W - Weeroc ASICs Evaluation System SN/PID: 17537			<a href="#">Details</a>
Ticket #TT159299	Status: Closed	Date: 26/09/2024	
Title: Roadflag function in v2495 Device: WV2495KAAAA - V2495 - Programmable Logic Unit PLUS SN/PID: 94			<a href="#">Details</a>
Ticket #TT159147	Status: Closed	Date: 29/08/2024	
Title: v2495 Device: WV2495KAAAA - V2495 - Programmable Logic Unit PLUS SN/PID: 94			<a href="#">Details</a>
Ticket #TT157634	Status: Closed	Date: 14/11/2023	
Title: Sci-compiler Petrioc Trigger (Block) Device: WDT5550WXXXX - DT5550W - Weeroc ASICs Evaluation System SN/PID: 17537			<a href="#">Details</a>
Ticket #TT157584	Status: Answered by customer	Date: 08/11/2023	
Title: Sci Compiler custom packet get data (Python) Device: WDT5550WXXXX - DT5550W - Weeroc ASICs Evaluation System SN/PID: 17537			<a href="#">Details</a>
Ticket #TT157561	Status: Closed	Date: 08/11/2023	
Title: Sci Compiler Custom Packet Device: WDT5550WXXXX - DT5550W - Weeroc ASICs Evaluation System SN/PID: 17537			<a href="#">Details</a>
Ticket #TT157528	Status: Closed	Date: 02/11/2023	
Title: LEMO.io input (bug) Device: WDT5550WXXXX - DT5550W - Weeroc ASICs Evaluation System SN/PID: 17537			<a href="#">Details</a>
Ticket #TT157499	Status: Closed	Date: 30/10/2023	
Title: Sci-compiler project for default firmware DT5550W board (Petrioc) Device: WDT5550WXXXX - DT5550W - Weeroc ASICs Evaluation System SN/PID: 17537			<a href="#">Details</a>
Ticket #TT157307	Status: Closed	Date: 26/09/2023	
Title: Sci Compiler v22.10.0.1 Download Device: SN/PID:			<a href="#">Details</a>
Ticket #TT157299	Status: Closed	Date: 22/09/2023	
Title: Sci Compiler license Device: SN/PID:			<a href="#">Details</a>
Ticket #TT157291	Status: Closed	Date: 21/09/2023	
Title: niusb3_core.dll Sci-compiler Device: WDT5550WXXXX - DT5550W - Weeroc ASICs Evaluation System SN/PID: 17537			<a href="#">Details</a>
Ticket #TT156210	Status: Closed	Date: 06/03/2023	
Title: Sci Compiler .dcp files Device: SN/PID:			<a href="#">Details</a>
Ticket #TT156206	Status: Open	Date: 06/03/2023	
Title: Sci Compiler custom HDL Device: SN/PID:			<a href="#">Details</a>



# Еще больше OpenSource



🔗 website [hdl-modules.com](https://hdl-modules.com) 📄 github [hdl-modules/hdl-modules](https://github.com/hdl-modules/hdl-modules) 📄 license [BSD 3-Clause](#)  
💬 chat [GitHub Discussions](#) 🟢 ci [passing](#)

The hdl-modules project is a collection of reusable, high-quality, peer-reviewed VHDL building blocks. It is released as open-source project under the very permissive BSD 3-Clause License.

This website contains human-readable documentation of the modules. To check out the source code, go to the [GitHub page](#).

The code is designed to be reusable and portable, while having a clean and intuitive interface. Resource utilization is always critical in FPGA projects, so these modules are written to be as efficient as possible. Using generics to enable/disable different features and modes means that resources can be saved when not all features are used. Some entities are very deliberately area optimized, such as the FIFOs, since they are used very frequently in FPGA projects.

More important than anything, however, is the quality. Everything in this project is peer reviewed, has good unit test coverage, and is proven in use in real FPGA designs. All the code is written with readability and maintainability in mind.

The following things can be found, at a glance, in the different modules:

- **axi**: AXI3/AXI4 Crossbars, FIFOs, CDCs, etc.
- **axi\_lite**: AXI-Lite Crossbars, FIFOs, CDCs, etc.
- **bfm**: Many BFM for simulating AXI/AXI-Lite/AXI-Stream.
- **common**: Miscellaneous, but useful, things that do not fit anywhere else.
- **fifo**: Synchronous and asynchronous FIFOs with AXI-stream-like handshake interface.
- **hard\_fifo**: Wrappers, with cleaner AXI-stream-like handshake interfaces, around hard FIFO primitives.
- **lfsr**: Maximum-length linear feedback shift registers for pseudo-random number generation.
- **math**: Some common math function implementations.
- **reg\_file**: A generic register file and a simulation support package for register operations.
- **resync**: CDC implementations for different signals and buses, along with proper constraints.
- **sine\_generator**: Professional sinusoid waveform generator (or DDS, NCO).

## На данный момент ограничен доступ



### Open Source, Vendor Independent VHDL Common Library

This library is a collection of common components, functions, and procedures used in CERN gateway projects. The scope of the library is to simplify and standardise the development of gatewares for CERN.

#### Structure

- **colibri.common** Common Functions
- **colibri.pipes** Pipes entities (Arbiter, Router, ...)
- **colibri.fileio** File Operations
- **colibri.memory** Memory Entities (FIFOs, RAMs)
- **colibri.comms** Utilities for Communications (scrambler, PRBS, ...)
- **colibri.interfaces** Bus and Stream Protocols Components (AXI, Avalon, Wishbone, ...)
- **colibri.io** Input Output protocols (UART, I2C, ...)
- **colibri.misc** Miscellaneous

Everything in this repository should be compiled under `colibri` library.

Testbenches are available in the `sim` directory, formal verification tests are available in the `fv` directory.

#### License

The content of this repository is licensed under CERN-OHL-W-V2.

#### How to contribute

Contributing in the form of code, feedback, ideas or bug reports are welcome. Code contributions are expected to have self-checking testbenches, formal verification tests, and pass the style checks. If there are any problems let us know.

Before doing any major changes we recommend creating an issue or chatting with us on mattermost to discuss first. In this way you do not get started on the wrong track and waste time.

#### Contributors

2023 - 2024 [@alperro](#) alberto.perro (at) cern.ch  
2024 [@mvodnik](#) mitja.vodnik (at) cern.ch



**FDF 2024**  
**FPGA Developers' Forum**  
*an open space to discuss FPGA design*

**1st meeting**  
**CERN, 11-13 June 2024**

**Organising Committee:**  
 Nicoló Vladi Biesuz - INFN, IT  
 Filiberto Bonini - CERN, CH  
 Andrea Borga - Oliscience, NL  
**Davide Cieri (co-chair) - Max-Planck-Institute for Physics, DE**  
 Christian Glaser - Uppsala University, SE  
**Francesco Gonnella (co-chair) - University of Birmingham, UK**  
 Evangelia Gousiou - CERN, CH  
 Christian Krieg - TU Wien, AT  
 Mathieu Saccani - CERN, CH  
 Paschalis Vichoudis - CERN, CH  
 Tom Williams - RAL, UK  
 Rui Zou - Cornell University, US

cern.ch/fdf      fdf@cern.ch



- Sharable HDL Cores
- Solutions to everyday digital design problems
- Algorithm implementation
- HDL development, verification, and simulation tools

High-Level Synthesis for Machine Learning	Nicolo Ghilmetti
30/7-018 - Kjell Johnsen Auditorium, CERN	16:15 - 16:45
Under the Canopy: Exploring Conifer for Low-Latency Decision Forests on FPGAs	Sioni Paris Summers
30/7-018 - Kjell Johnsen Auditorium, CERN	16:45 - 17:15
UVVM - An Introduction to the world's fastest growing FPGA verification methodology	Espen Tallaksen
30/7-018 - Kjell Johnsen Auditorium, CERN	17:15 - 17:55
LoCod: an open-source hardware/software co-design tool for SoC/FPGA	Florent Manni
30/7-018 - Kjell Johnsen Auditorium, CERN	17:55 - 18:15

16:00	Convenient and reliable clock domain crossings, using scoped constraints and reusable blocks	Lukas Vik
	30/7-018 - Kjell Johnsen Auditorium, CERN	15:40 - 16:20
	COLIBRI: Towards a CERN-wide common cores library	Alberto Perro
	30/7-018 - Kjell Johnsen Auditorium, CERN	16:20 - 16:50
17:00	CERN control group cores and tools	Tristan Gingola
	30/7-018 - Kjell Johnsen Auditorium, CERN	16:50 - 17:20
	Fast Monitoring of FPGA algorithms using SpyBuffers	Iacopo Longarini
	30/7-018 - Kjell Johnsen Auditorium, CERN	17:20 - 17:50
18:00	The BondMachine Project	Mirko Mariotti et al.
	30/7-018 - Kjell Johnsen Auditorium, CERN	17:50 - 18:20

09:00	YML2HDL tool	Thiago Costa De Paiva
	30/7-018 - Kjell Johnsen Auditorium, CERN	09:00 - 09:20
	Automatic code generation for managing the firmware and software for configuration/status registers and memories in	Anna Malgorzata Kulinska
	Assertion-Based Formal Debugging During RTL Development	N. Engelhardt
10:00		
	30/7-018 - Kjell Johnsen Auditorium, CERN	09:40 - 10:15
	Open source formal verification with SymbiYosis	Yann Thoma
	30/7-018 - Kjell Johnsen Auditorium, CERN	10:15 - 10:45
11:00	Coffee Break	
	30/7-018 - Kjell Johnsen Auditorium, CERN	10:45 - 11:15
	Becoming vendor agnostic with the help of model-based source code generation	Alexander Wirthmüller
	30/7-018 - Kjell Johnsen Auditorium, CERN	11:15 - 11:50
12:00	HDL on git (Hog)	Nordin Aranzabal Barrio
	30/7-018 - Kjell Johnsen Auditorium, CERN	11:50 - 12:20
	Summary of 1st FDF meeting	Dr Rui Zou
	30/7-018 - Kjell Johnsen Auditorium, CERN	12:20 - 12:40
	Closing Remarks	Dr Francesco Gonnella
	30/7-018 - Kjell Johnsen Auditorium, CERN	12:40 - 12:50

# Fast Machine Learning for Science (Workshop)

**Fast Machine Learning for Science**

Real-time and accelerated ML for fundamental sciences

**Imperial College London**

25-28 September 2023

**Scientific Committee**

- Thea Aarrestad (ETH Zurich)
- Javier Duarte (UCSD)
- Phil Harris (MIT)
- Burt Holzman (Fermilab)
- Scott Hauck (U. Washington)
- Shih-Chieh Hsu (U. Washington)
- Sergo Jindariani (Fermilab)
- Mia Liu (Purdue University)
- Allison McCarn Deiana (Southern Methodist University)
- Mark Neubauer (U. Illinois Urbana-Champaign)
- Jennifer Ngadiuba (Fermilab)
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**PURDUE UNIVERSITY**

**FAST MACHINE LEARNING FOR SCIENCE**

Oct. 15 to 18, 2024. Purdue University

*Fast ML meets fundamental sciences, quantum information science, semiconductors*

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Спасибо за внимание