VII КОНФЕРЕНЦИЯ FPGA/RTL/Verification

FPGA-Systems 2024.2

Что нового у BMTI?

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Пример правильного взаимодействия комьюнити и дистрибьютора

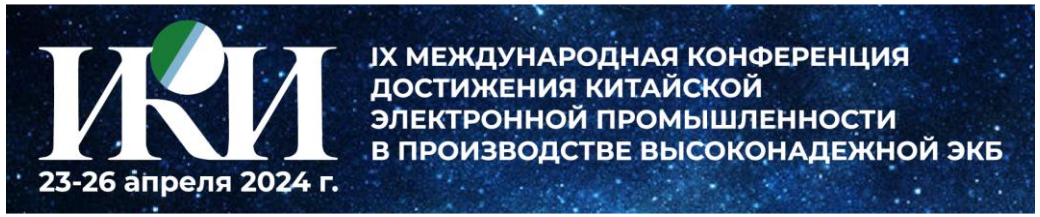
Записи прошлых выступлений АО Эпсилон

Обзор ПЛИС/FPGA производства BMTI, КНР // Денис Кижа

FPGA Systems

Высоконадежная ЭКБ Пекинского института...

FPGA Systems



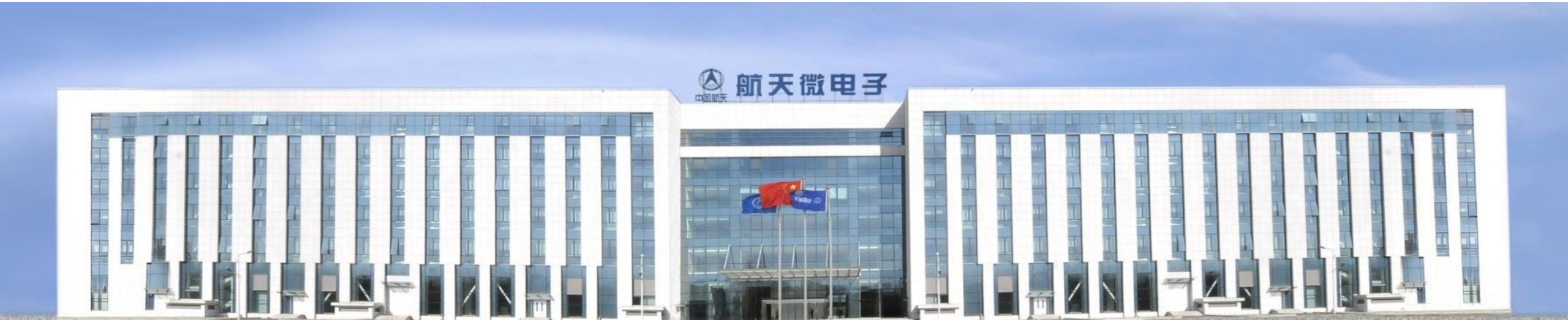
Ежегодная конференция, проводимая компанией «Эпсилон».
Записи всех докладов и презентации доступны в телеграм канале @AOEPSILON

00

Эпсилон и BMTI: кто это?

Информация о BMTI

- основан в 1994 году
- входит в состав КААЭТ при Китайской Корпорации Аэрокосмической науки и техники
- Инвестируется государством в сфере разработки ЭРИ для космоса
- 900+ сотрудников
- Fabless компания, основной Foundry – SMIC (Шанхай



BMTI делает не только ПЛИС

Трансиверы

RF и MMCI

Память

АЦП / ЦАП

Системы-в-Корпусе

Системы-на-Кристалле

Шины и интрефейсы

Микропроцессоры

Микросхемы дискретной логики

Управление питанием

ПЛИС / FPGA

... и много чего ещё

Спросите «Эпсилон»
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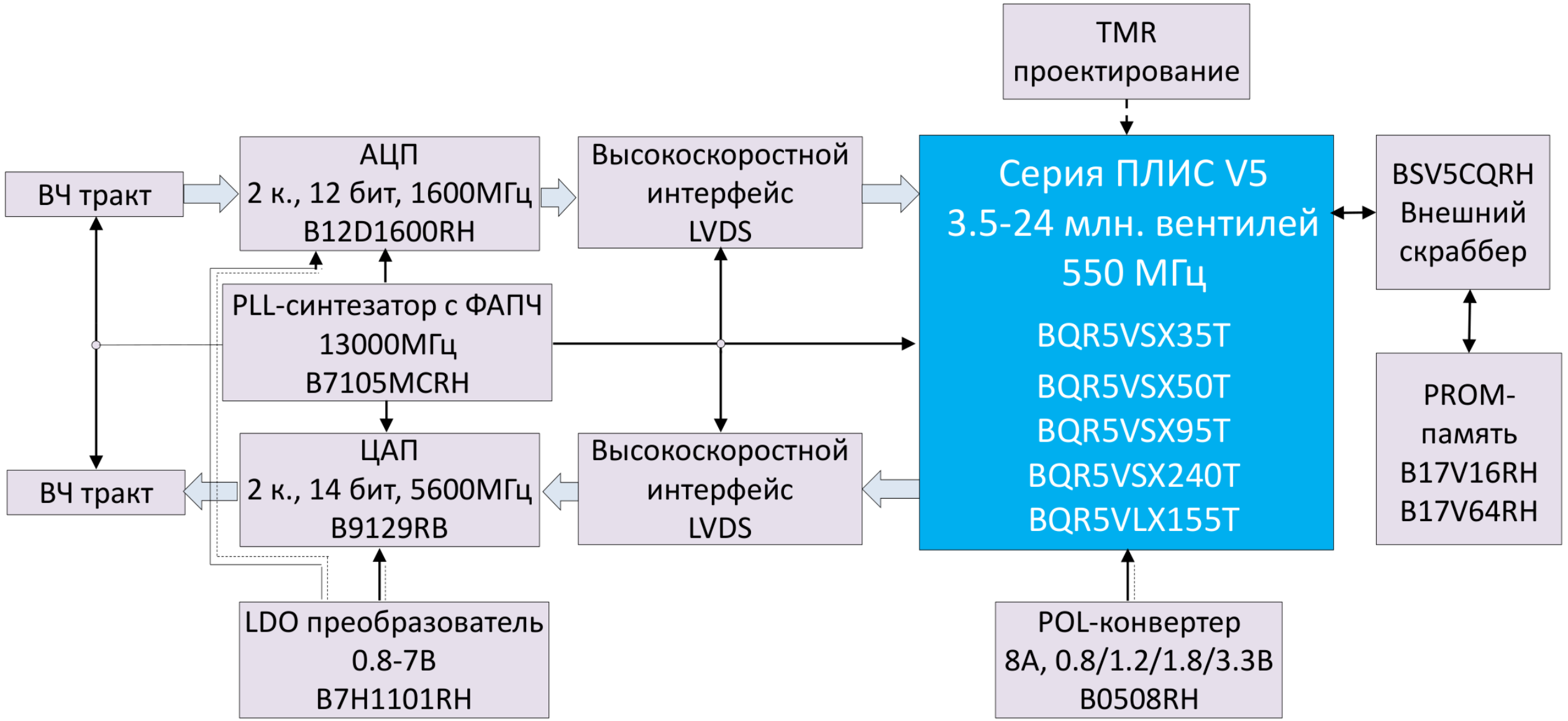
Пример задачи, решенной в рамках экосистемы BMTI



01

ПЛИС, Системы-в-Корпусе и Системы-на-Кристалле

Радстойкая линейка ПЛИС, СнК и СвК

BQRVU3P
BQRVU9P

86.2Million Gates
250Million Gates

2024

Радстойкая линейка ПЛИС, СнК и СвК

BQRVU3P
BQRVU9P

86.2Million Gates
250Million Gates

***BQRVU13P**

378Million Gates

2024

Радстойкая линейка ПЛИС, СнК и СвК

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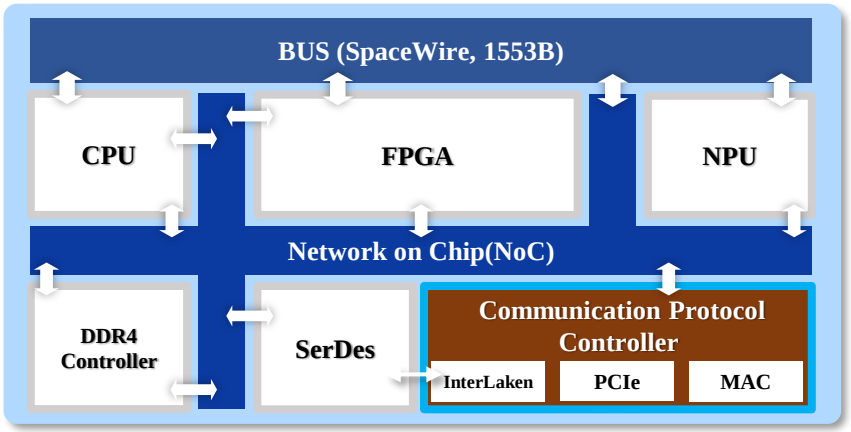
378Million Gates

***HXBV02A1**

86.2Million Gates

2024



Радстойкая линейка ПЛИС, СнК и СвК

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BQRVU9P

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250Million Gates

2024

***BQRVU13P**

378Million Gates

***HXBV02A1**

86.2Million Gates

***BQR7Z045**
***BQR7Z100**

35Million Gates
44Million Gates

2025

Радстойкая линейка ПЛИС, СнК и СвК

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***HXBV02A1**

86.2Million Gates

***BQR7Z045**
***BQR7Z100**

35Million Gates
44Million Gates

2025

***BQRZU28DR**
***BQRZU48DR**

86.2Million Gates

2026

High-level (-40-15 : 85+40)

Кто понял, тот понял

BQVU3P/9P
BQ7A50T/100T

86/258 Million Gates, 775MHz
5/10 Million Gates, 933MHz

2024

High-level (-40-15 : 85+40)

BQVU3P/9P
BQ7A50T/100T

86/258 Million Gates, 775MHz
5/10 Million Gates, 933MHz

2024

2024.6

BQVU3P
BQ7A50T/100T

High-level (-40-15 : 85+40)

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BQ7A50T/100T

86/258 Million Gates, 775MHz
5/10 Million Gates, 933MHz

BQVU9P

2024 **2024.6** **2025**

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BQ7A50T/100T

High-level (-40-15 : 85+40)

BQVU3P/9P
BQ7A50T/100T

86/258 Million Gates, 775MHz
5/10 Million Gates, 933MHz

BQVU9P

2024 | **2024.6** | **2025** | **2025.6**

BQVU3P
BQ7A50T/100T

BQ7Z045
BQ7Z100

High-level (-40-15 : 85+40)

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86/258 Million Gates, 775MHz
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BQVU9P

BQVU13P
BQZU28DR/48DR

2024 | **2024.6** | **2025** | **2025.6** | **2026**

BQVU3P
BQ7A50T/100T

BQ7Z045
BQ7Z100

Industrial

BCVU3P/9P
BC7A50T/100T

86/258 Million Gates, 775MHz
5/10 Million Gates, 933MHz

2024

Industrial

BCVU3P/9P
BC7A50T/100T

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2024

2024.6

BCVU3P
BC7A50T/100T

Industrial

BCVU3P/9P
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BCVU9P

2024 **2024.6** **2025**

BCVU3P
BC7A50T/100T

Industrial

BCVU3P/9P
BC7A50T/100T

86/258 Million Gates, 775MHz
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BCVU9P

2024 | **2024.6** | **2025** | **2025.6**

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BCVU9P

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BCZU28DR/48DR

2024 | **2024.6** | **2025** | **2025.6** | **2026**

BCVU3P
BC7A50T/100T

BC7Z045
BC7Z100

02

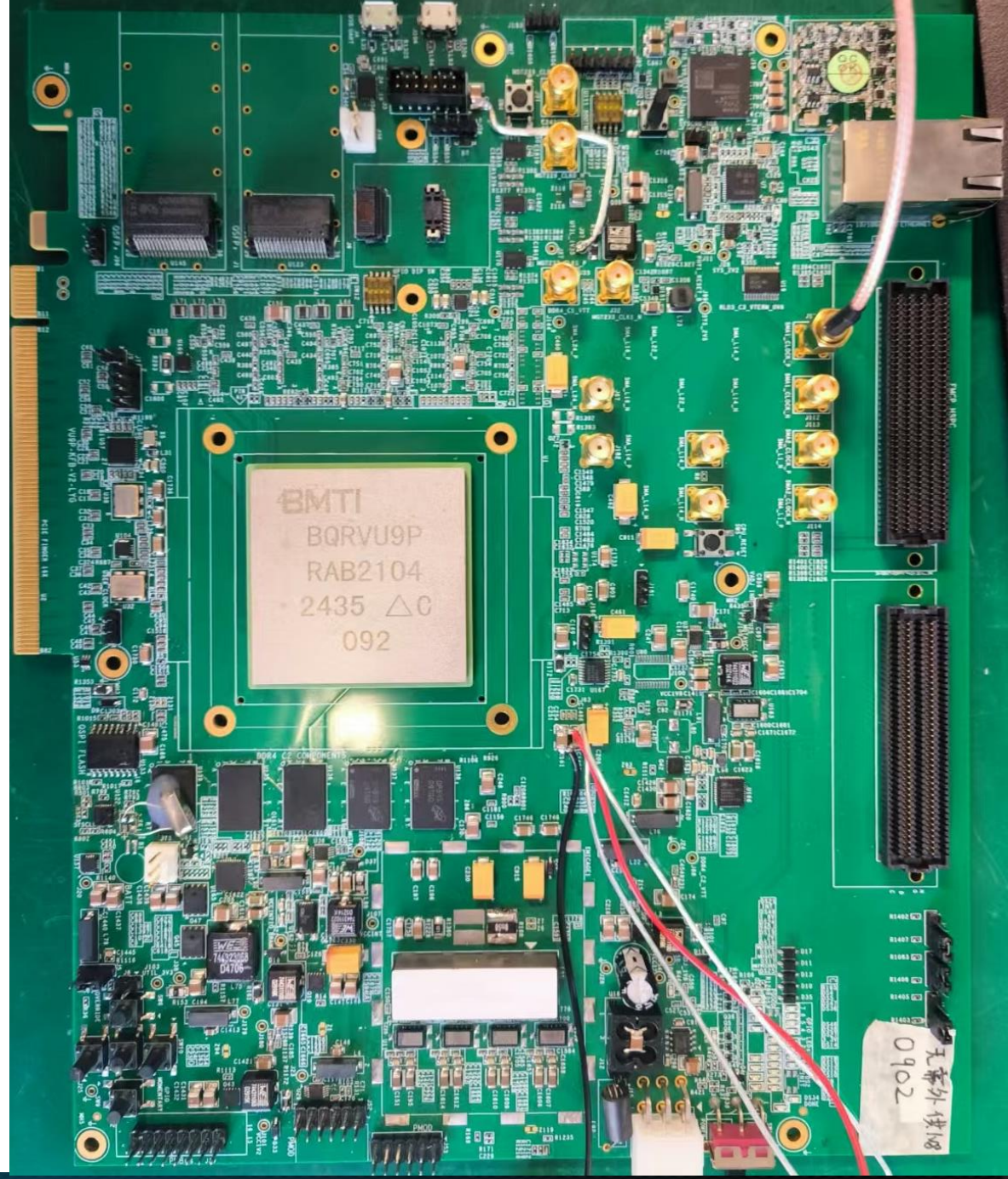
Обновление линейки отладочных плат

BQVU3PBG1517 (Radiation Hardened)

- Transceivers up to 128x33G can achieve 8.4 Tb of serial bandwidth
- Medium speed grade 2,666 Mb/s DDR4
- Standard PCIe Gen3x16
- Support program configuration using QSPI mode
- Support Micro-B for connecting to computer serial port communication
- FMC interface for function extension and customer customization requirements, providing test programs
- Demonstrates DDR IP software, PCIe XDMA transfer, fiber ibert test

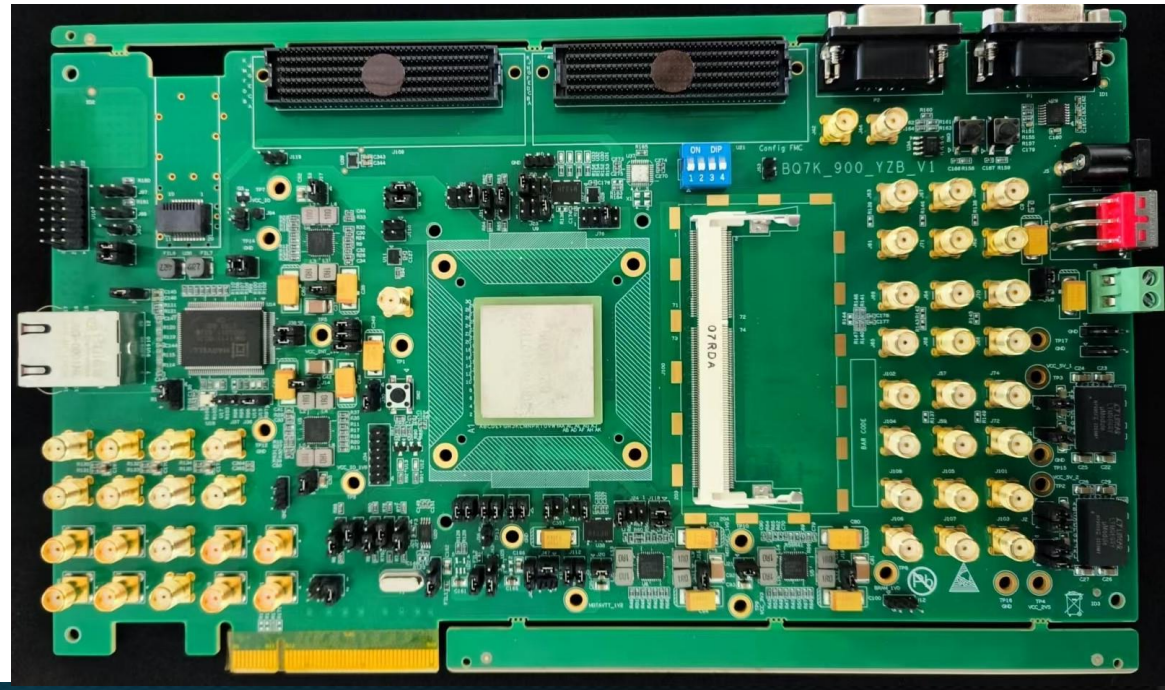
BQRVU9P (Radiation Hardened)

- Transceivers up to 128x33G can achieve 8.4 Tb of serial bandwidth
- Medium speed grade 2,666 Mb/s DDR4
- Standard PCIe Gen3x16
- Support program configuration using QSPI mode
- Support Micro-B for connecting to computer serial port communication
- FMC interface for function extension and customer customization requirements, providing test programs
- Demonstrates DDR IP software, PCIe XDMA transfer, fiber ibert test



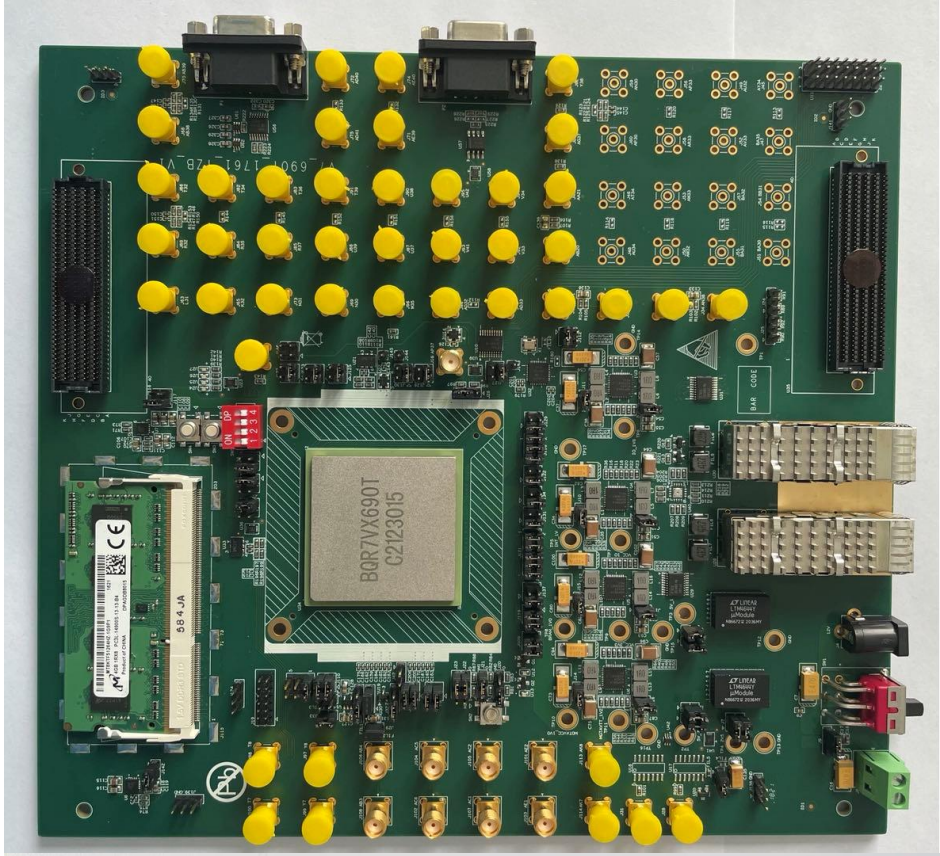
BQR7K325T
BQR7K410T
(Radiation Hardened)

- **Memory：** 1.5V DDR3 memory module slot, support MT8KTF51264HZ-1G9P1 memory module, memory module capacity 4Gb.
- **Clock and reset:** provide single-ended 80MHz, differential 200MHz clock input, provide 1 pair of SMA differential clock input interface (2 pairs of differential IO can be used as SMA clock input); 1 global reset button.
- **IO and high-speed interface:** provide 11 pairs of differential IO and 2 GTX interfaces.
- **Interface protocol:** support SFP, RS485, RS232 interface protocol.
- **Configuration mode:** support JTAG online programming and debugging, support the use of FMC daughter board master/slave SPI, master/slave Select MAP, master/slave serial, master/slave BPI mode configuration.
- **Dimensions：** 26.6mm X 15.7mm。



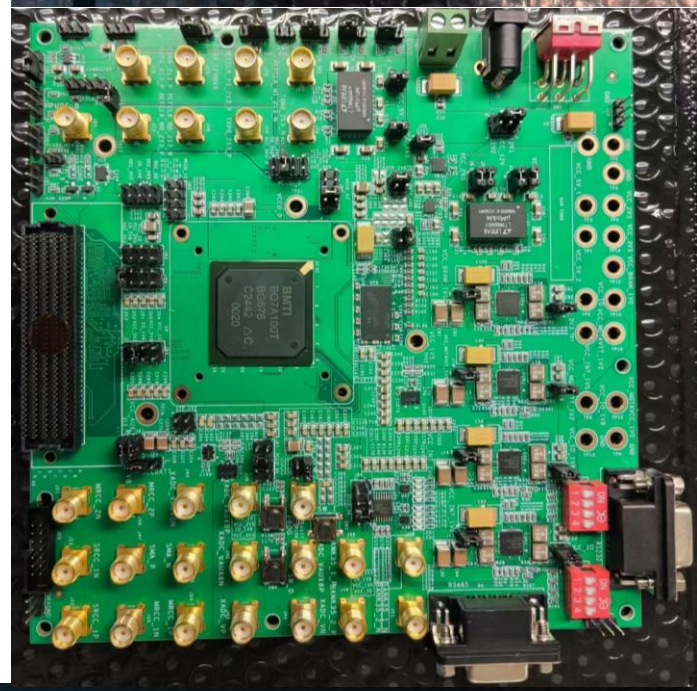
BQR7VX690T-1761
BQR7VX690T-1927
(Radiation Hardened)

- **Memory：** 1.5V DDR3 memory module slot, support MT8KTF51264HZ-1G9P1 memory module, memory module capacity 4Gb.
- **Clock and reset:** provide single-ended 80MHz, differential 200MHz clock input, provide 1 pair of SMA differential clock input interface (8 / 4 pairs of differential IO can be used as SMA clock input); 2 global reset button.
- **IO and high-speed interface:** provide 24 / 9 pairs of differential IO and 2 GTH interfaces.
- **Interface protocol:** support SFP, RS485, RS232 interface protocol.
- **Configuration mode:** support JTAG online programming and debugging, support the use of FMC daughter board master/slave SPI, master/slave Select MAP, master/slave serial, master/slave BPI mode configuration.

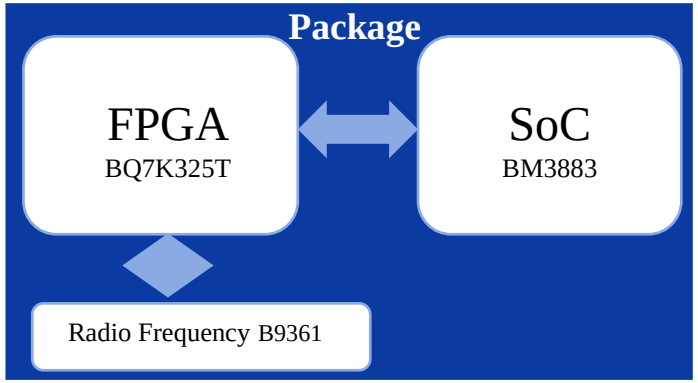


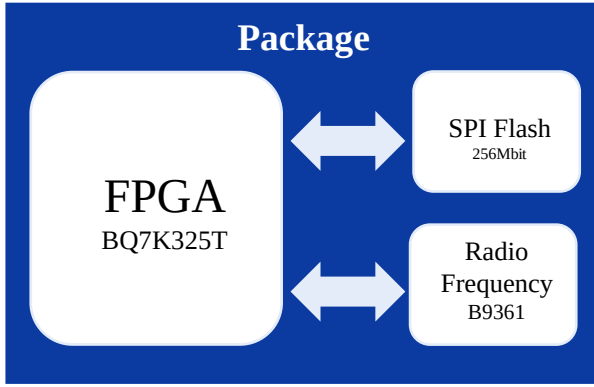
BQ7A50T
BQ7A100T
(High-level)

- GTP Transceivers up to 6.25Gbps
- Medium speed grade 800 Mb/s DDR3
- Configuration interface FMC
- RS485 and RS232
- XADC input IO
- Support program configuration using QSPI, BPI mode and so on
- Demonstrates DDR IP software, PCIe XDMA transfer, fiber



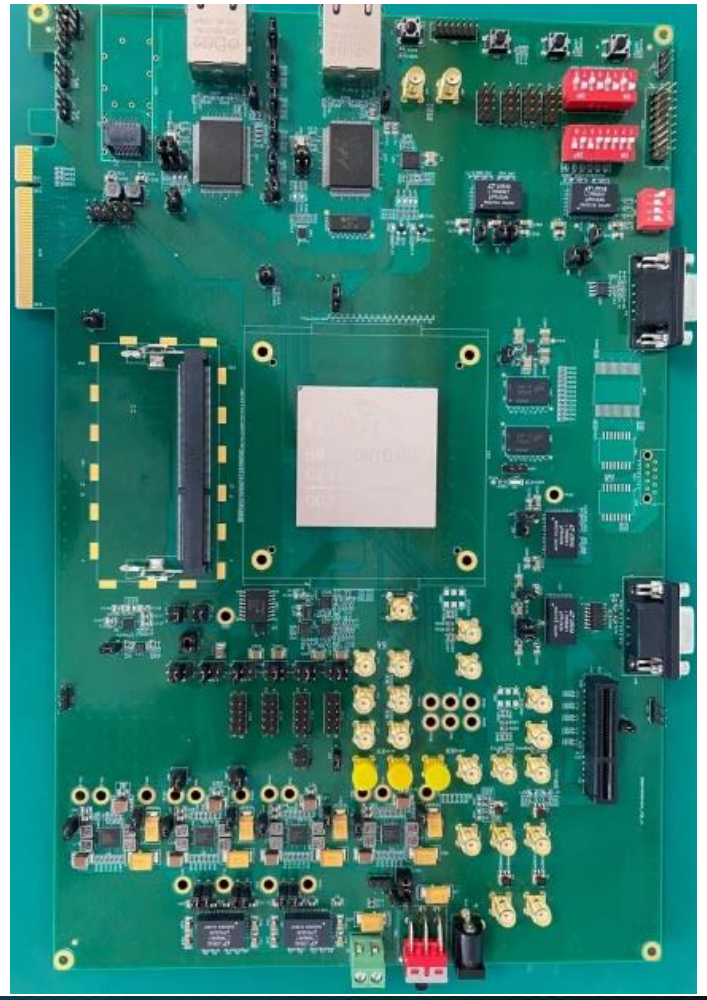
HXBQ01A1
HXBQ03A1
(High-level)





- **Memory**：1.5V DDR3 memory slot is configured on the FPGA end and supports MT8KTF51264HZ-1G9P1 memory with 4GB memory capacity.
- **Clock and reset:** provide single-ended 80MHz, differential 200MHz clock input.
- **Interface protocol:** support RS232/RS485 interface protocol
  - **HXBQ01A1** Support CPU serial port debugging.

- **Configuration mode:** support JTAG online programming debugging, support the SPI Flash configuration.
- **Dimensions**：212.73mm X 310mm



*HXBV02A1 – будет в керамике

03

Прораммное обеспечение HT-FDS

BMTI HongTu – ещё не Vivado

HongTu(HT) series software is a powerful suite of tools for FPGA and SoPC application development. HongTu provides

- an easy-to-use IDE covering all necessary components for FPGA and embedded system development
- a range of additional high-reliable and high-security features

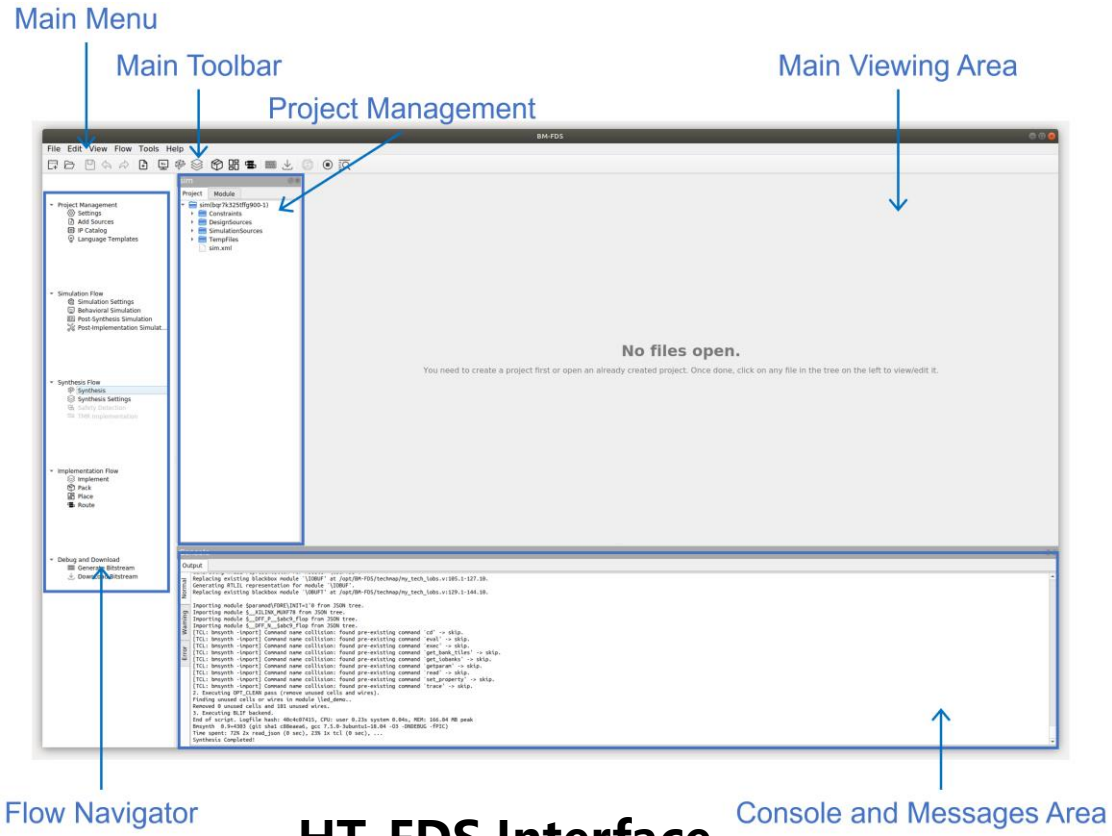
These capabilities facilitate users from aerospace, defense and industry to accelerate development and enhance reliability in specific application area.

鸿途
HongTu

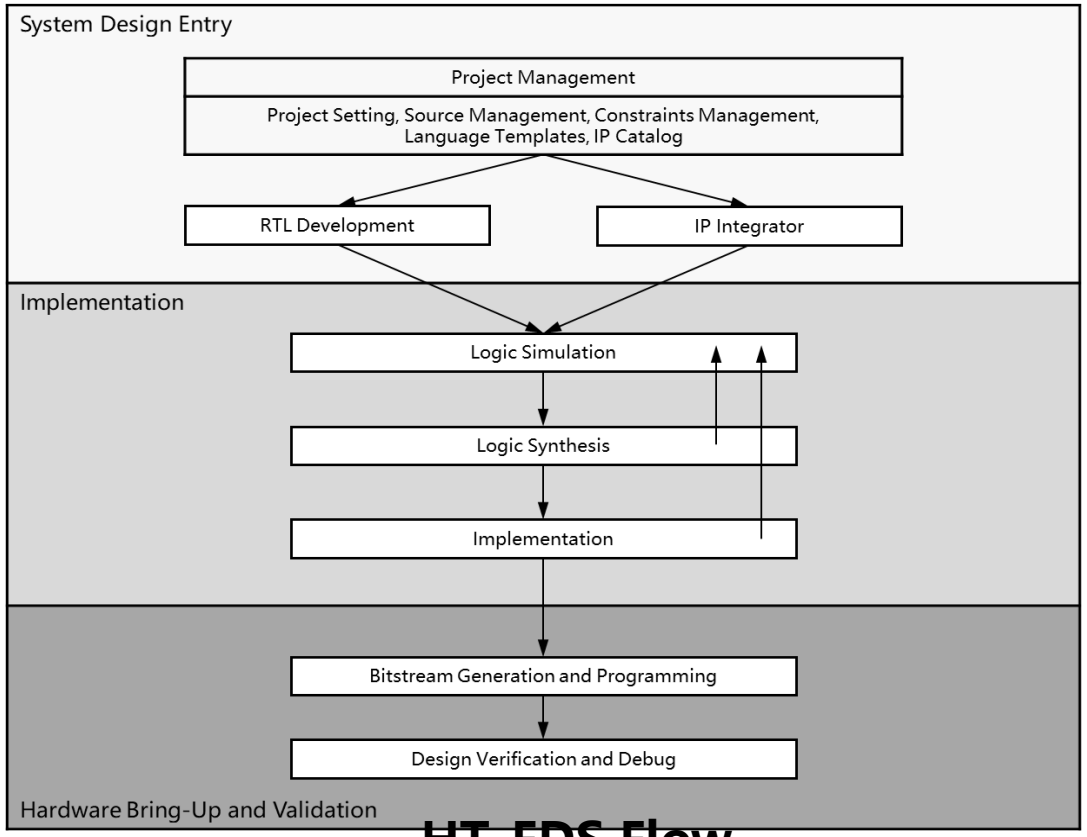
Product	Type	Function
HT-FDS	FPGA Design Suite	FPGA Full-Flow development
HT-Studio	General Embedded IDE	SoPC application development
HT-TMR	TMR Tool	Soft error sensitivity assessment
HT-FI	Fault Injection Tool	Soft error mitigation optimization
HT-TD	Trojan Detection Tool	Malicious logic detection

HT-FDS: FPGA Full-Flow Development Tool

HT-FDS is an independent full-flow development tool for BMTI FPGAs. HT-FDS supports all FPGA implementation flows from HDL code writing to bitstream downloading, and is characterized by complete functionality, efficient algorithms, IP friendliness, good scalability and compatibility.



HT-FDS Interface



HT-FDS Flow

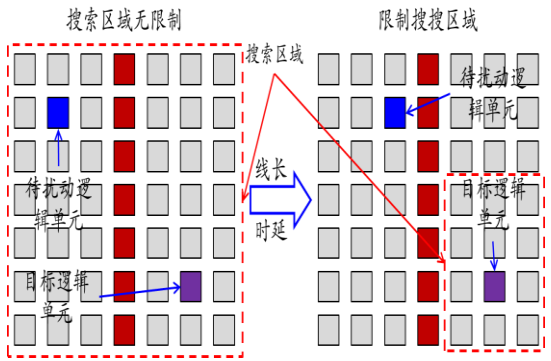
HT-FDS Features

Full Function

Project Management
IP Integrator
Synthesis
Map
Place
Route
Logic Simulation
Bitstream Generation
Bitstream Download
Design Debug
TMR

Advanced Algorithms

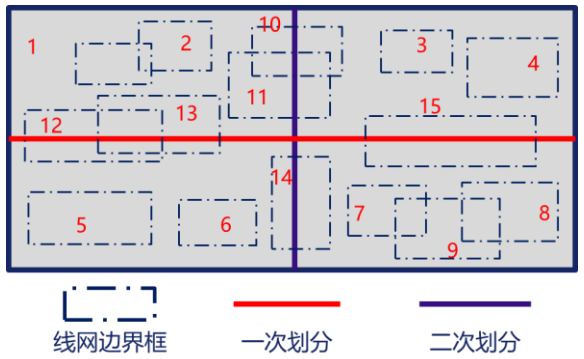
- ✓ HT-FDS employs techniques such as **reinforcement learning** and **hybrid wire meshing** to outperform Vivado (2020) 28.1%



Reinforcement Learning based Placement

High Scalability

- ✓ HT-FDS can add support for **custom architecture FPGAs**



Routing based on Efficient Parallelization Strategies

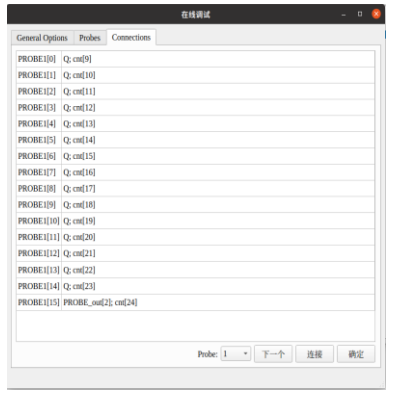
Rich IP Support

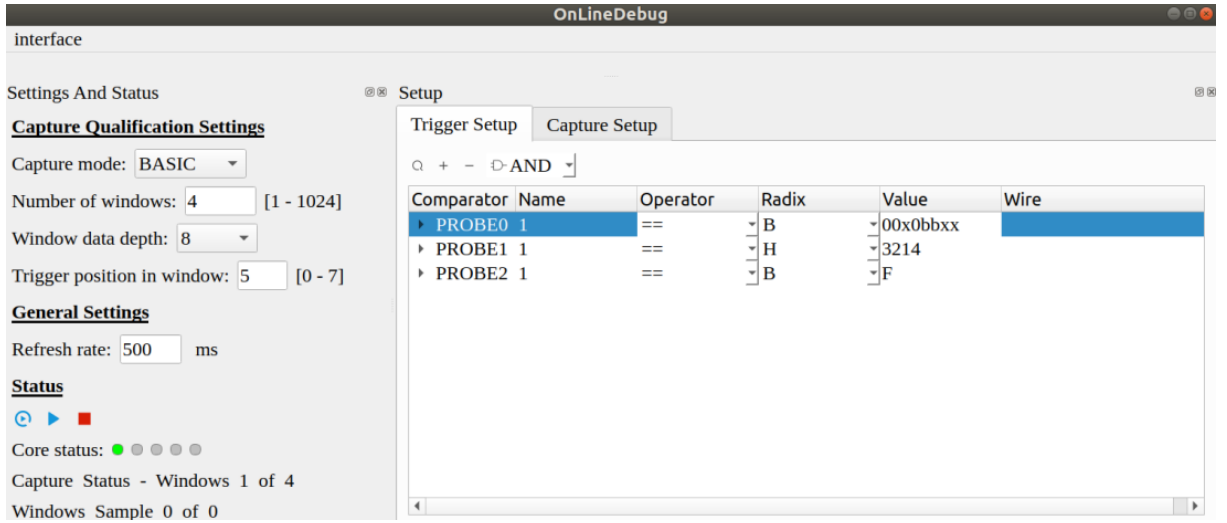
- ✓ HT-FDS supports a rich set of computing and interface IP cores

IP Catalog
DSP
BRAM
MATH
DDR
AXI
FIFO
RISC-V
ILA
SEM

HT-FDS Special Feature 1: Integrated Logic Analyzer Core

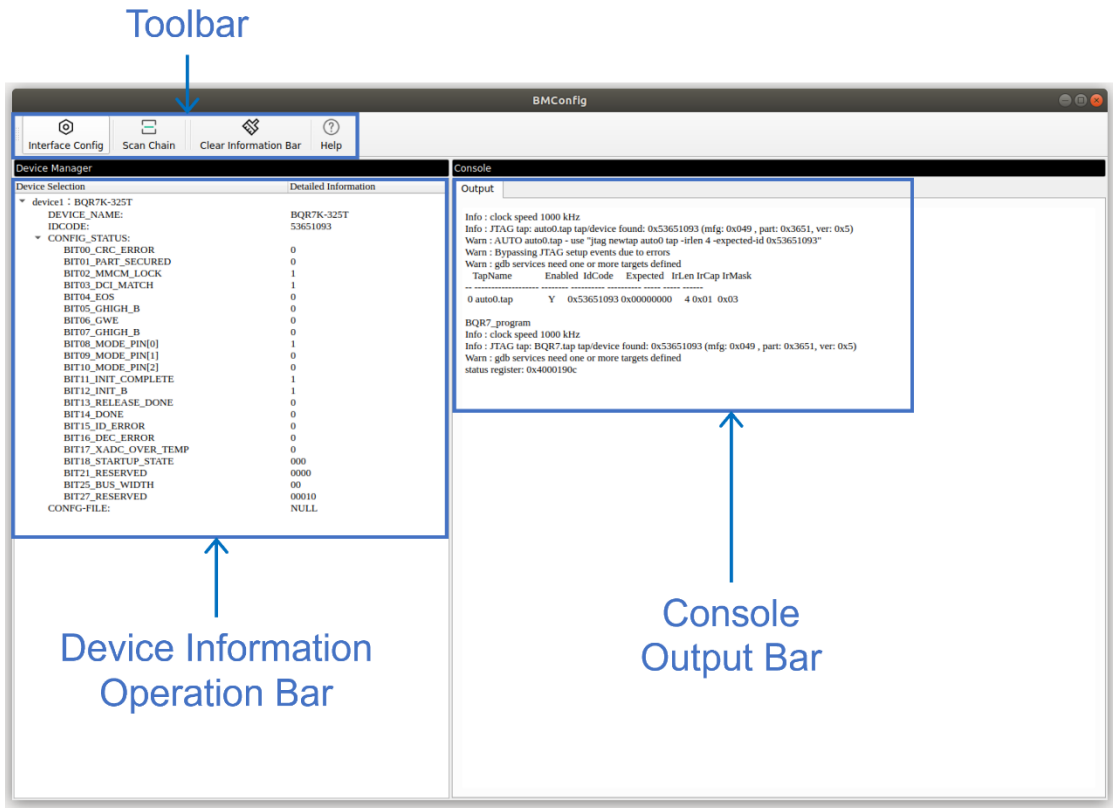
- ✓ Support 5 series, 7 series FPGAs.
- ✓ **Flexible usage**: instantiated in RTL code / inserted in post-synthesis netlist of the HT-FDS design flow.
- ✓ **Powerful performance**: configured to select 1,024 probes each of width ranging from 1 to 4,096. The maximum number of samples is 131,072.
- ✓ **Multiple trigger setup**: support boolean trigger equations and edge transition triggers.
- ✓ **Capture model setup**: store signals on demand for monitoring specific period of internal signals.





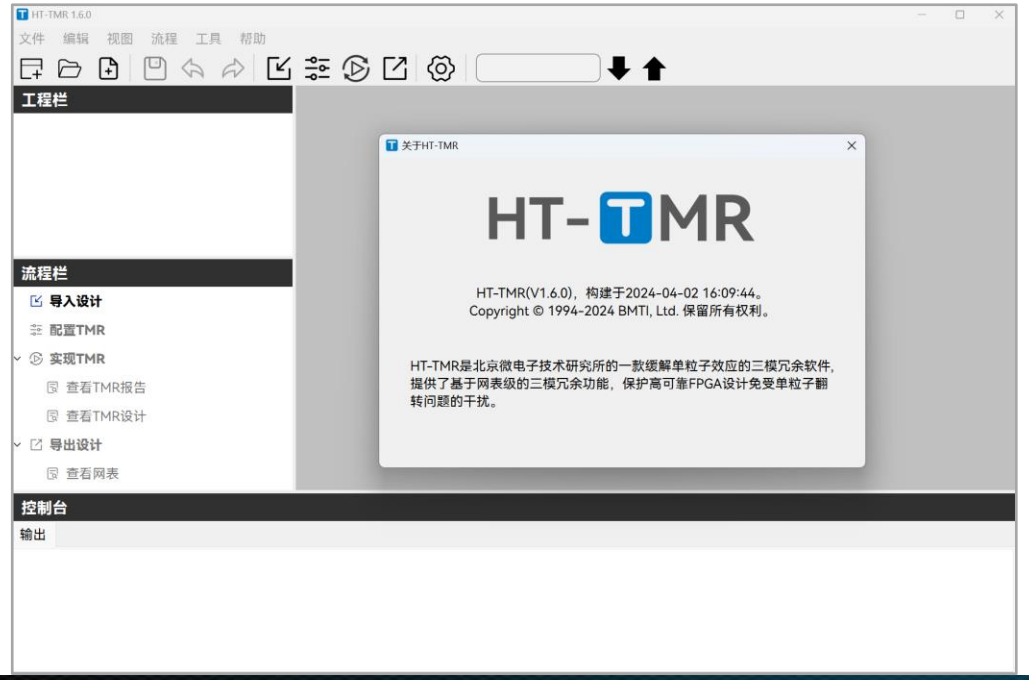
HT-FDS Special Feature 3: Configuration Download Tool

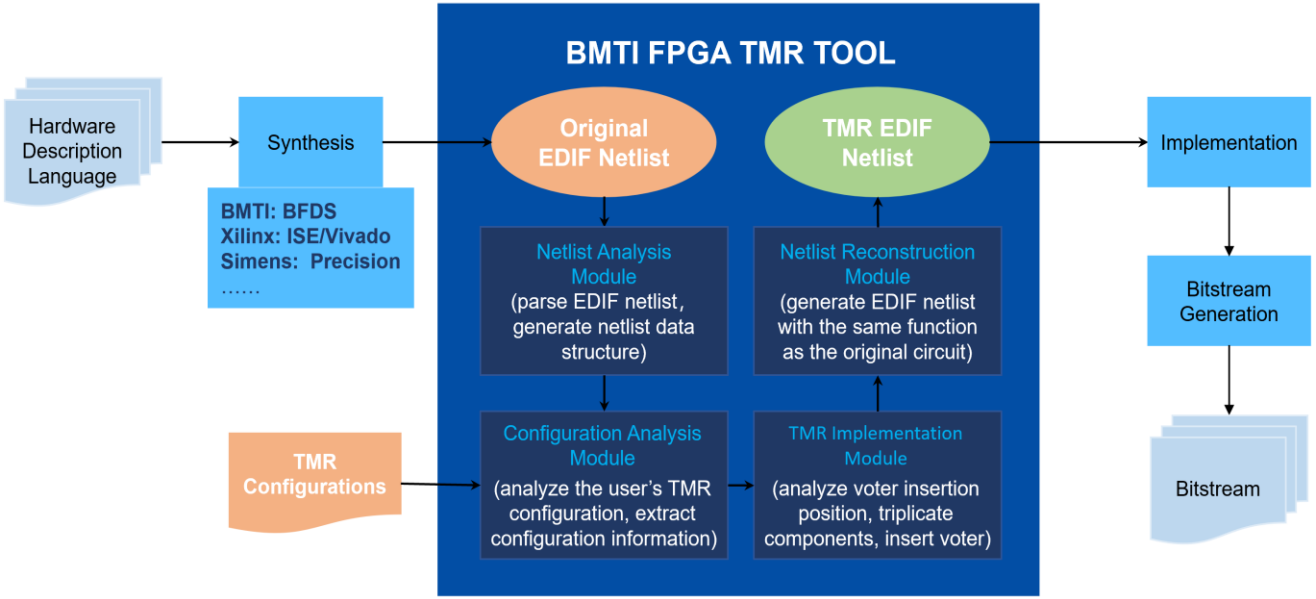
- ✓ All target devices in the JTAG chain can be automatically scanned after power-up and configured with target information.
- ✓ Compatible with Xilinx platform-cable USB in addition to BMTI cable USB support.
- ✓ User-defined interface profiles can be integrated.



HT-FDS Special Feature 4: HT-TMR Tool

- ✓ Automatically insert TMR into BMTI/Xilinx FPGA designs to mitigate SEU.
- ✓ Support **EDIF** format netlist design.
- ✓ Provide designers with complete control over how their designs are triplicated through **LTMR\DTMR\GTMR\CTMR**.
- ✓ Increase designer productivity by reducing errors and speeding TMR implementation.
- ✓ Competent to replace **Xilinx TMRTool** and **Siemens Precision Hi-Rel** tool.





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https://aoepsilon.ru/

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Сайт комьюнити
fpga-systems.ru

Стопроцентная вероятность вопроса про тайминги

Static Timing Analysis accuracy: customers do not trust on 100% for Vivado reports since BMTI FPGA has different technology?

- BMTI FPGA has been designed with accurate delay simulation for each cell and path during the design process, which can meet the specifications of Xilinx FPGA and satisfy the results in Vivado reports.